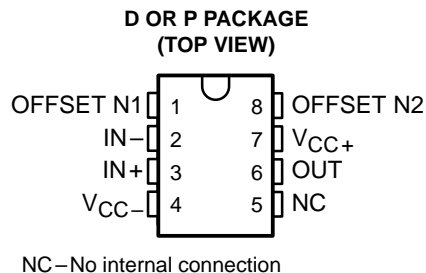


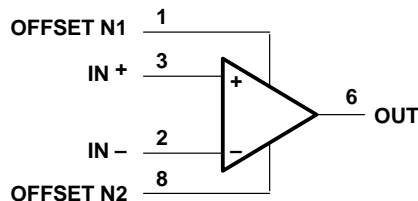
OP07C, OP07D, OP07Y PRECISION OPERATIONAL AMPLIFIERS

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- Low Noise
- No External Components Required
- Replaces Chopper Amplifiers at a Lower Cost
- Single-Chip Monolithic Fabrication
- Wide Input Voltage Range
0 to ± 14 V Typ
- Wide Supply Voltage Range
 ± 3 V to ± 18 V
- Essentially Equivalent to Fairchild μ A714 Operational Amplifiers
- Direct Replacement for PMI OP07C and OP07D



symbol



description

These devices represent a breakthrough in operational amplifier performance. Low offset and long-term stability are achieved by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation. The true differential input, with a wide input voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range. The OP07 is unsurpassed for low-noise, high-accuracy amplification of very low-level signals.

These devices are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	150 μ V	OP07CD OP07DD	OP07CP OP07DP	OP07Y

The D package is available taped and reeled. Add the suffix R to the device type (e.g., OP07CDR). The chip form is tested at T_A = 25°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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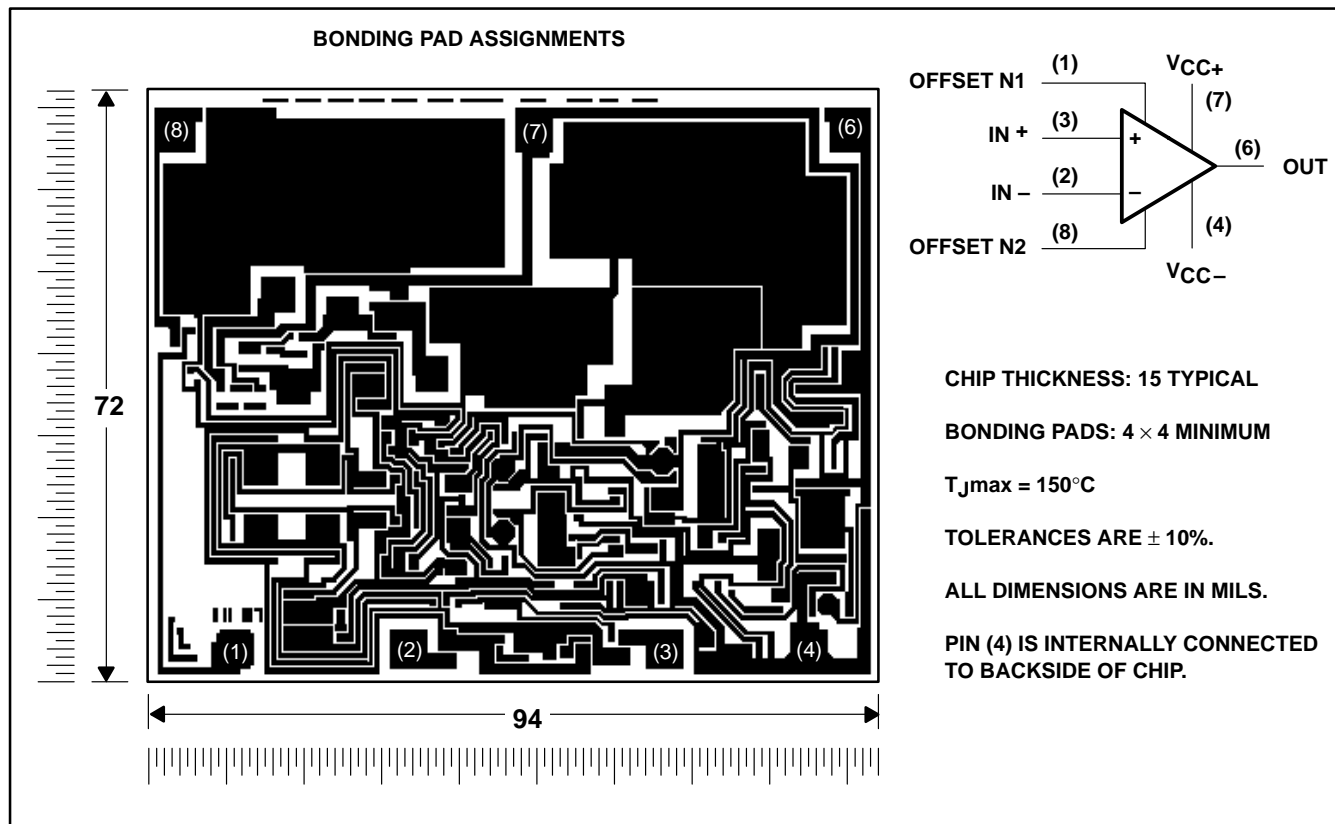
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OP07Y chip information

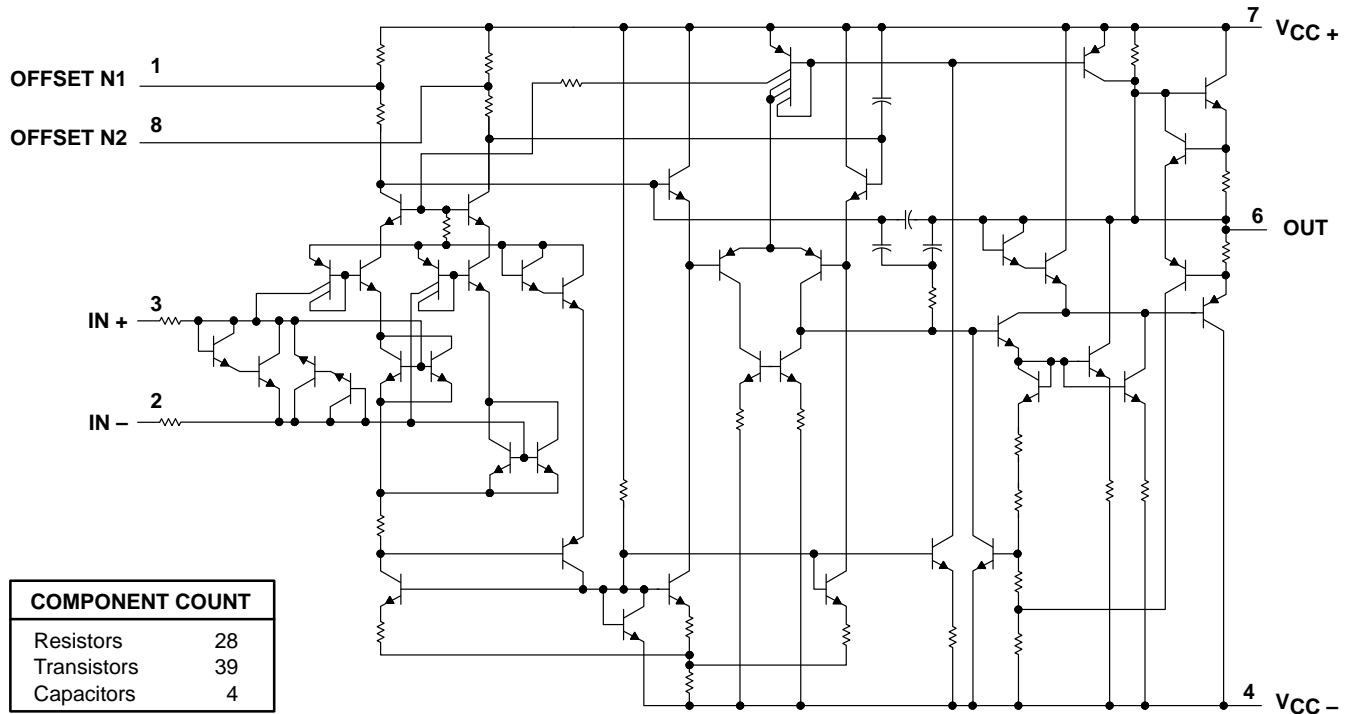
These chips, properly assembled, display characteristics similar to the OP07. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



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schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-}	-22 V
Differential input voltage (see Note 2)	± 30 V
Input voltage, V_I (either input, see Note 3)	± 22 V
Duration of output short circuit (see Note 4)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	500 mW
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

- NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential voltages are at IN+ with respect to IN-.
 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
 4. The output may be shorted to ground or either power supply.
 5. For operation above 64°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		± 3	± 18	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 15$ V	-13	13	V
Operating free-air temperature, T_A		0	70	°C

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electrical characteristics at specified free-air temperature, $V_{CC} \pm = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TA	OP07C			OP07D			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C	60	150	60	150	60	150	μV
α_{VIO} Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	0°C to 70°C	85	250	85	250	85	250	$\mu\text{V}/^\circ\text{C}$
Long-term drift of input offset voltage	See Note 6	0°C to 70°C	0.5	1.8	0.7	2.5	0.7	2.5	$\mu\text{V}/\text{mo}$
Offset adjustment range	$R_S = 20\ \text{k}\Omega$, See Figure 1	25°C	± 4		± 4		± 4		mV
I_{IO} Input offset current		25°C	0.8	6	0.8	6	0.8	6	nA
α_{IIO} Temperature coefficient of input offset current		0°C to 70°C	1.6	8	1.6	8	1.6	8	nA
I_{IB} Input bias current		0°C to 70°C	12	50	12	50	12	50	pA/°C
α_{IIB} Temperature coefficient of input bias current		25°C	± 1.8	± 7	± 2	± 12	± 2	± 12	nA
V_{ICR} Common-mode input voltage range		0°C to 70°C	± 2.2	± 9	± 3	± 14	± 3	± 14	nA
V_{OM} Peak output voltage	$R_L \geq 10\ \text{k}\Omega$	0°C to 70°C	18	50	18	50	18	50	pA/°C
	$R_L \geq 2\ \text{k}\Omega$	25°C	± 13	± 14	± 13	± 14	± 13	± 14	V
	$R_L \geq 1\ \text{k}\Omega$	0°C to 70°C	± 13	± 13.5	± 13	± 13.5	± 13	± 13.5	V
	$R_L \geq 2\ \text{k}\Omega$	25°C	± 12	± 13	± 12	± 13	± 12	± 13	V
	$V_{CC} \pm = \pm 3\ \text{V}$, $V_O = \pm 0.5\ \text{V}$, $R_L \geq 500\ \text{k}\Omega$	0°C to 70°C	± 11.5	± 12.8	± 11.5	± 12.8	± 11.5	± 12.8	V
	$V_O = \pm 10\ \text{V}$, $R_L = 2\ \text{k}\Omega$	25°C	± 12		± 12		± 12		V
A_{VD} Large-signal differential voltage amplification		0°C to 70°C	± 11	± 12.6	± 11	± 12.6	± 11	± 12.6	V/mV
B_1 Unity-gain bandwidth		25°C	100	400	100	400	100	400	MHz
r_i Input resistance		25°C	120	400	120	400	120	400	M Ω
CMRR Common-mode rejection ratio		0°C to 70°C	100	400	100	400	100	400	dB
kSVS Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{IC} = \pm 13\ \text{V}$, $R_S = 50\ \Omega$	25°C	0.4	0.6	0.4	0.6	0.4	0.6	$\mu\text{V}/\text{V}$
	$V_{CC} \pm = \pm 3\ \text{V}$ to $\pm 18\ \text{V}$, $R_S = 50\ \Omega$	25°C	8	33	7	31	7	31	$\mu\text{V}/\text{V}$
	$V_O = 0$, No load	0°C to 70°C	100	120	94	110	94	110	mW
	$V_{CC} \pm = \pm 3\ \text{V}$, $V_O = 0$, No load	25°C	97	120	94	106	94	106	mW
		25°C	7	32	7	32	7	32	mW
		0°C to 70°C	10	51	10	51	10	51	mW
		25°C	80	150	80	150	80	150	mW
		25°C	4	8	4	8	4	8	mW

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise noted.
NOTE 6: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first thirty days of operation.

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operating characteristics, $V_{CC\pm} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITION [†]	OP07C			OP07D			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	10.5			10.5			$\text{nV}/\sqrt{\text{Hz}}$
	$f = 100\text{ Hz}$	10.2			10.3			
	$f = 1\text{ kHz}$	9.8			9.8			
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }10\text{ Hz}$	0.38			0.38			μV
I_n Equivalent input noise current	$f = 10\text{ Hz}$	0.35			0.35			$\text{pA}/\sqrt{\text{Hz}}$
	$f = 100\text{ Hz}$	0.15			0.15			
	$f = 1\text{ kHz}$	0.13			0.13			
$I_{N(PP)}$ Peak-to-peak equivalent input noise current	$f = 0.1\text{ Hz to }10\text{ Hz}$	15			15			pA
SR Slew rate	$R_L \geq 2\text{ k}\Omega$	0.3			0.3			$\text{V}/\mu\text{s}$

[†] All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise noted.

electrical characteristics, $V_{CC\pm} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITION [†]	OP07Y			UNIT
		MIN	TYP	MAX	
V_{IO} Input offset voltage	$R_S = 50\ \Omega$	60		150	μV
Long-term drift of input offset voltage	See Note 6	0.5			$\mu\text{V}/\text{mo}$
Offset adjustment range	$R_S = 20\text{ k}\Omega$, See Figure 1	± 4			mV
I_{IO} Input offset current		0.8		6	nA
I_{IB} Input bias current		± 2	± 12		nA
V_{ICR} Common-mode input voltage range		± 13	± 14		V
V_{OM} Peak output voltage	$R_L \leq 10\text{ k}\Omega$	± 12	± 13		V
	$R_L \leq 2\text{ k}\Omega$	± 11.5	± 12.8		
	$R_L \leq 1\text{ k}\Omega$	± 12			
A_{VD} Large-signal differential voltage amplification	$V_{CC\pm} = \pm 3\text{ V}$, $V_O = \pm 0.5\text{ V}$, $R_L \leq 500\text{ k}\Omega$	400			
	$V_O = \pm 10\text{ V}$, $R_L = 2\text{ k}\Omega$	120	400		
B_1 Unity-gain bandwidth		0.4	0.6		MHz
r_i Input resistance		7	31		$\text{M}\Omega$
CMRR Common-mode input resistance	$V_{IC} = \pm 13\text{ V}$, $R_S = 50\ \Omega$	94	110		dB
k_{SVS} Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 3\text{ V to } \pm 18\text{ V}$, $R_S = 50\ \Omega$	7	32		$\mu\text{V}/\text{V}$
P_D Power dissipation	$V_O = 0$, No load	80	150		mW
	$V_{CC\pm} = \pm 3\text{ V}$, $V_O = 0$, No load	4	8		

NOTE 6: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first thirty days of operation.



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operating characteristics, $V_{CC\pm} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONST	OP07Y			UNIT
		MIN	TYP	MAX	
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$		10.5		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$		10.3		
	$f = 0.1\text{ Hz to }10\text{ Hz}$		9.8		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }10\text{ Hz}$		0.38		μV
I_n Equivalent input noise current	$f = 10\text{ Hz}$		0.35		$\text{pA}/\sqrt{\text{Hz}}$
	$f = 100\text{ Hz}$		0.15		
	$f = 1\text{ kHz}$		0.13		
$I_{N(PP)}$ Peak-to-peak equivalent input noise current	$f = 0.1\text{ Hz to }10\text{ Hz}$		15		pA
SR Slew rate	$R_L = 2\text{ k}\Omega$		0.3		$\text{V}/\mu\text{s}$

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise noted.

APPLICATION INFORMATION

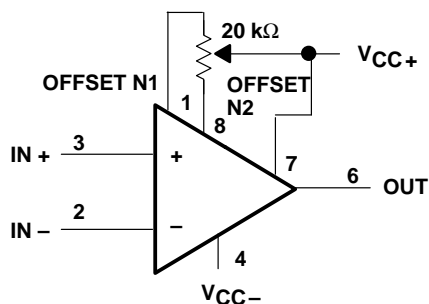


Figure 1. Input Offset Voltage Null Circuit

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