Bt868/869

Interfacing the Bt868/869 VGA Encoder to a Graphics Controller Application Note

Rockwell
Semiconductor Systems

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Introduction

This application note should be used as a supplement to the *Bt868/869 Datasheet* and reviewed after successful installation of the Bt868EVK demo kit. The steps required to interface the Rockwell Bt8686/869 VGA Encoder to a PCI or AGP graphics controller are described. It is intended for engineers and marketeers from graphics controller vendors, Rockwell Field Applications Engineers, Account Managers, and Sales Representatives. The purpose is to provide all the necessary knowledge for conversion of the Creative Labs' Graphics Exxtreme card + Bt868 ISA card (and ***Bt868 COCKPIT*** software) from a demonstration tool into a piece of development hardware and software. After review of this document, the end user should be able to electrically connect the existing Bt868EVK encoder card directly to the controller vendor's target graphics card. In this configuration, the controller acts as the I^2C master to the I^2C slave Bt868/Bt869 VGA Encoder. This arrangement also allows the Bt868 to directly receive the controller's pixel clock and digital pixel data. Finally, the Bt868 is able to transmit a reference pixel clock (CLKO) and transmit or receive the Horizontal Sync (HSYNC*), Vertical Sync (VSYNC*), and BLANK* signals that denote the start of an analog line, an analog field, and the blanked regions respectively.

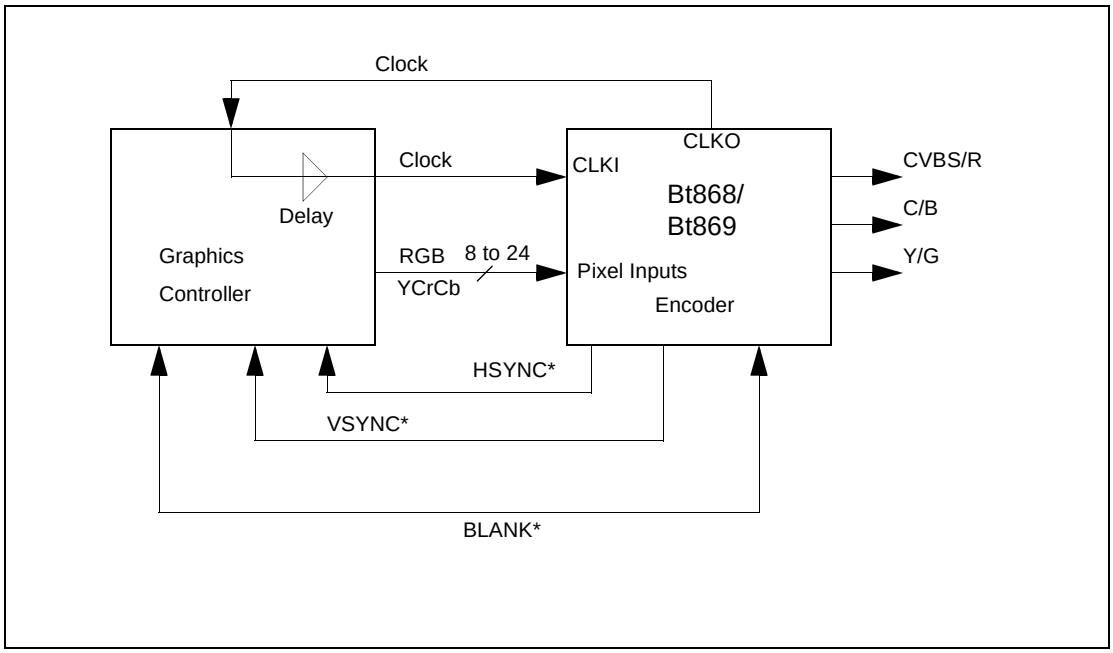
Please see the end of this application note for a complete schematic of the BT868EVK Reference Design card for the Bt868 or Bt869.

NOTE: The Bt869 is a Bt868 with additional circuitry for the Macrovision 7 anti-copy algorithm. Any interested companies must obtain a license from *Macrovision* (http://www.macrovision.com:80/) to use the Bt869 VGA Encoder, with Macrovision capability, from Rockwell.

Description of Possible Physical Interfaces

As stated in the *Bt868/869 Datasheet*, the Bt868 encoder can be operated as either a timing master or a timing slave. In master mode, HSYNC*, VSYNC*, CLKO, and BLANK* are generated by the encoder as outputs. For slave mode, the graphics controller must provide these signals. In either case, the timing must adhere to Figure 4-2 or 4-3 in the data sheet. All of the possible physical interfaces are illustrated in this section.

Figure 1. Master Mode



Referring to Figure 1, notice that the Bt868 has 3 output lines (HSYNC*, VSYNC*, and CLKO) connected directly to the graphics controller for master mode. A minimum of 9 inputs are also required for this configuration. One signal should be used for CLKI and at least 8 for the pixel lines. The amount of inputs could grow to 25 if 24-bit non-multiplexed RGB mode is used by the designer.

Rockwell defines master mode to exist when the graphics controller can accept the encoder's reference clock and send back that same clock, albeit a delayed version, with the pixel data transitions synchronized to this signal's rising and falling (or rising only) edges. This would be done via the Bt868's clock output (CLKO) and clock input (CLKI) respectively.

Reasons for BLANK signal*

In either master, pseudo-master, or slave mode, the Bt868/869 does not have to receive the BLANK* signal.

However, for graphics controllers that meet **all** of the following criteria:

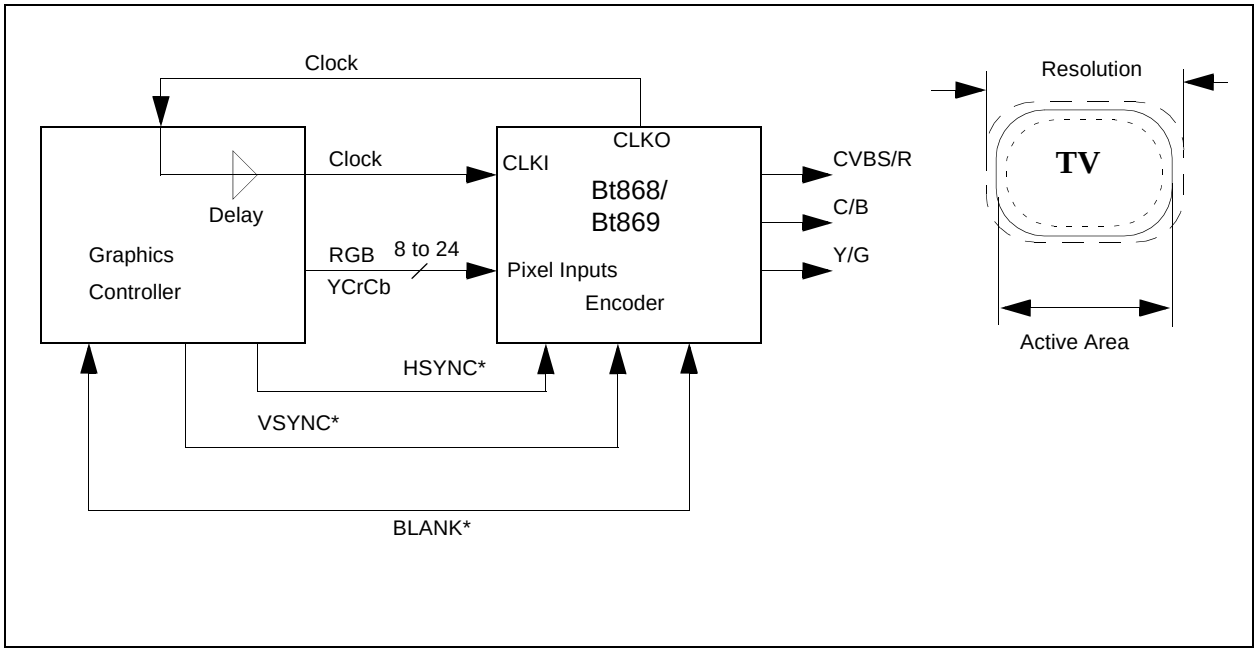
- Operate the encoder in master mode where the Bt868 transmits HSYNC*, VSYNC*, and CLKO
- Possess resolution of HSYNC* detection greater than 1 pixel clock wide

then, a BLANK* signal would definitely be necessary.

A typical example would be a graphics controller that detects the HSYNC* signal only at character clock boundaries. Since character clocks are typically 8 or 9 pixel clocks in duration, several pixel clocks can elapse between the arrival of the HSYNC* signal and the detection of that signal by the graphics controller. The graphics controller will start providing active pixels relative to its detection of the HSYNC* signal, so there are several pixel clocks of variability in the location of the first active pixel relative to the HSYNC* signal. Therefore, the encoder cannot rely on pixel

clock counting to determine the location of the first active pixel, and must receive a signal from the graphics controller that carries the information. Thus, the BLANK* signal is required in the physical interface to indicate the exact location of the first active pixel on each line.

Figure 2. Pseudo-Master Mode



Referring to Figure 2, notice that the Bt868 only has 1 output line (the reference clock; CLKO) connected directly to the graphics controller for pseudo-master mode. For this configuration, a minimum of 11 inputs are required. One line each for CLKI and the Video Timing signals (HSYNC* and VSYNC*) plus the 8 pixel lines. In most configurations, BLANK* is not necessary (see note below).

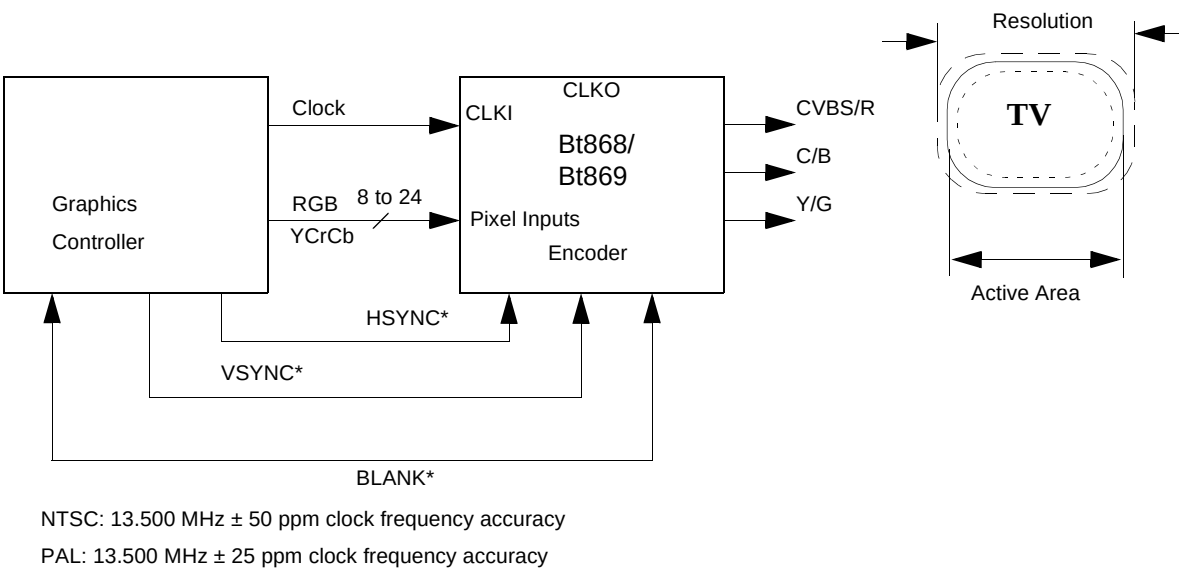
The amount of inputs could grow to a maximum of 28 if 24-bit non-multiplexed RGB mode is used by the designer to send data to the Bt868 VGA Encoder.

NOTE: In pseudo-master mode, BLANK* can be used as an input to the Bt868 or an output from the Bt868. If blanking is not being used whatsoever in the physical interface, the BLANK* pin must still be configured in software as an output for valid NTSC or PAL video output. To do this, set the EN_BLANKO bit equal to 1 (i.e., bit D7 of register 0xC6). EN_BLANKO will then configure the BLANK* pin as an output.

If the BLANK* pin is an output from the Bt868, the encoder's internal counters define the active regions where input data will be captured. If the BLANK* pin is configured as an input (i.e., EN_BLANKO = 0), then the BLANK* signal's functionality is deferred to the particular EN_DOT (bit D6 of register 0xC6) setting. If EN_DOT is set (= 1), then the rising edge of the incoming BLANK* signal will be used to indicate where the first active pixel occurs. After the location of the first pixel is known by the encoder, the Bt868's internal counters will define the timing when active pixels will be captured from the rising edge of BLANK* onwards until the end of the active data. If EN_DOT is reset (= 0), then the input BLANK* signal from the graphics controller will solely define the region where active pixel data will be captured.

The BLANK feature, used in the Bt868 interface, might not be supported by other non-Rockwell VGA Encoders.

Figure 3. Slave Mode



NTSC: 13.500 MHz ± 50 ppm clock frequency accuracy

PAL: 13.500 MHz ± 25 ppm clock frequency accuracy

NOTE: Graphics controller must be able to generate highly accurate, low jitter (less than 1 ns) clock to utilize this interface.

Referring to Figure 3, notice that the Bt868 has 0 output lines connected directly to the graphics controller. For this configuration, a minimum of 11 inputs are required for slave mode. One line each for CLKI and the Video Timing signals (HSYNC* and VSYNC*) plus the 8 pixel lines.

The amount of inputs could increase to a maximum of 28 if 24-bit non-multiplexed RGB mode is used by the designer to send data to the VGA Encoder.

This is the least desirable hardware configuration for the Bt868 interface to a graphics controller. Normally, the Bt868 generates the video timing signals, CLKO, FIELD, and color subcarrier from the main clock frequency (i.e., 13.500 MHz) being injected into the encoder via the XTALIN and XTALOUT inputs. Being in master mode ensures that a highly accurate internal clock frequency is being used because a 13.500 MHz frequency, with low tolerance, is injected to the encoder via the crystal and XTAL circuit. Forcing the Bt868 to accept the clock from an external source dictates that the Bt868 derives the color subcarrier frequency (either ~3.58 MHz for NTSC or ~4.43 MHz for PAL) from the graphics controller clock (CLKI). Typically, these devices use crystals with tolerances from 100-200 ppm. Frequency deviations in this range prevent a television from effectively demodulating the color analog video being created by the Bt868. Even with an accurate clock, problems could still exist with the amount of jitter present on the CLKI signal. In summary, slave mode should be chosen only when no other interfaces are possible for the graphics controller.

Using Bt868EVK to Connect the Bt868 to Target Graphics Controller

Rockwell has an evaluation kit available for customers of the Bt868 Flicker Filter Encoder. This kit is called the Bt868EVK and is comprised of two hardware cards. The first is the Creative Labs' Graphics Blaster Exxtreme PCI card with the Permedia 2 controller. This is a low-cost, good-performance, target graphics card used to provide the Windows environment with a display on the PC monitor. The other hardware that comes with the kit is called the Bt868 ISA card that utilizes an ISA slot to provide power and ground to the Bt868 itself. The two cards are connected together via a VMI 1.4 style interface with supplied ribbon cables. Please note that Rockwell has determined that Creative's implementation of VMI 1.4 might differ slightly from the official VESA specification. Please exercise caution if using this EVK as a starting point for your own design with a VMI 1.4 video peripheral bus. See the schematics in Appendix B.

The Bt868 ISA card is designed to be both an evaluation and development unit. Two prototyping areas have been included on the Bt868 ISA card, which can be used to connect to other devices or to another graphics controller once the user has gained sufficient familiarity with this system.

In addition to the prototyping area, the EVK contains the following items:

- Installation instructions
- Beta Bt868 drivers
- ***Bt868 COCKPIT*** program to allow full user control over the Bt868 registers
- Reference schematics of Bt868 ISA card
- Reference board Bill of Materials
- *Bt868/869 Datasheet* and Bt868 errata sheet (on CDROM)
- Documentation on Creative Labs' Graphics Exxtreme PCI Card (Creative Labs' drivers should not be installed.)
- Bt868 ISA card
- Creative Labs' Graphics Blaster Exxtreme PCI Card
- 2 ribbon cables, (40 pin and 26 pin) to connect the Bt868 ISA card to the Graphics Exxtreme PCI Card (The connectors are labeled JP2 and JP1 respectively on the Bt868 ISA card.)

The appropriate signal names and connections that can be made from the target graphics controller to the Bt868 are also listed on the Bt868's JP3 header. This header is about 7 cm long by 1 cm wide. The Bt868's signals are exposed on the card as a 2-pin-wide by 26-pin-long header located adjacent to the VMI connectors on the Bt868. The JP3 and JP4 headers might not be installed on every Bt868 ISA card.

Installation of Bt868 COCKPIT Program with the 3D Labs Permedia2

With this simple hardware development platform now set up (i.e., Bt868 ISA and Graphics Blaster card), tasks on the software side will be addressed.

From our efforts to create a complete development environment, Rockwell Semiconductor has created a Windows '95 application and named it ***Bt868 COCKPIT***. This program's sole purpose is to give the design engineer the ability to write to any of the Bt868/869's internal registers or bits. If a VM700 Analog Video Signal monitor, as well as an NTSC or PAL TV is used, the effect of each register or bit manipulation can easily been seen on the television output image and on the video signal itself.

To get ***Bt868 COCKPIT***, order a Bt868EVK kit from your local Rockwell sales office. The ***Bt868 COCKPIT*** application is now shipped as part of the Bt868EVK software. Before using it, first install the Bt868 ISA card and the PCI Creative Labs' Permedia2 based Graphics Blaster Exxtreme as specified in the Installation Instructions. Version 1.02 (and later) of ***Bt868 COCKPIT*** only functions properly with the Graphics Blaster PCI board based on the Permedia2 graphics controller from 3D Labs. The application itself will be loaded into the C:/Bt868 directory upon installation. The source code for this application was last compiled in June 1998.

Although ***COCKPIT*** is used with the Permedia2 graphics controller, it is possible to modify the "i2c_skel.def" and "i2c_skel.cpp" files and recompile to make a new type of ***COCKPIT*** application. This customized version could issue I^2C writes to the encoder from another graphics controller made by a different vendor. To receive directions on how to modify and rebuild the software files appropriately, please contact your local Rockwell Field Applications Engineer.

The original "i2c_skel.def" and "i2c_skel.cpp" files, as well as other helpful Bt868/Bt869 related information can be retrieved from the dedicated Bt868 FTP site at:

ftp://bt868:tvout@ftp.brooktree.com/

Using with MIIC-201 Adapter and Version 0.21 of Bt868 COCKPIT

For those users familiar with the older Bt868EVM board and the RS232C to I^2C adapter from MCC (MIIC-201), it is still acceptable to use the I-PORT connector on the Bt868EVK with ***COCKPIT***. Once the P2 connector on the Bt868 is plugged into the male end of the I^2C cable then the corresponding I^2C write commands will be transmitted from the RS232C to I^2C adapter attached to the PC to the device. For reference, the latest version of this type of ***Bt868 COCKPIT*** software available is version 0.21. This version again requires installation of the MIIC-201 adapter.

You may skip to the end of this section if using the Bt868EVK kit without the MIIC-201. Only follow these instructions if utilizing the MIIC-201 adapter and version 0.21 of ***Bt868 COCKPIT*** for I^2C writes.

The only necessary addition to be made is to attach the iPort™ Windows I^2C Host Adapter (model MIIC-201) from Micro Computer Control Corporation to the PC's COM1 serial port. COM2 can be selected as well within ***Bt868 COCKPIT*** application, but ***COCKPIT*** looks for COM1 as the default setting.

A picture of the MIIC-201 iPort is shown in Figure 4.

Basically, the MIIC-201 adapter turns the Windows-based PC Serial Port into an I^2C Master. This adapter does require the PC's serial port to be a standard 25-pin male connector. If only 9 pins are available, then a DB25 male to DB9 female connector will need to be purchased and mated up to a 9-pin male COM1 serial connector.

NOTE: The graphics controller vendor is advised not to load the software contained on the diskette shipped by MCC. This particular software does not release the I^2C bus after each write, which is a problem for the ***Bt868 COCKPIT*** application. Furthermore, the power adapter

for the MCC-201 adapter should not be used either as the voltage level is 5 V. This differs from the low voltage I^2C bus for the Bt868, which is 3.3 V.

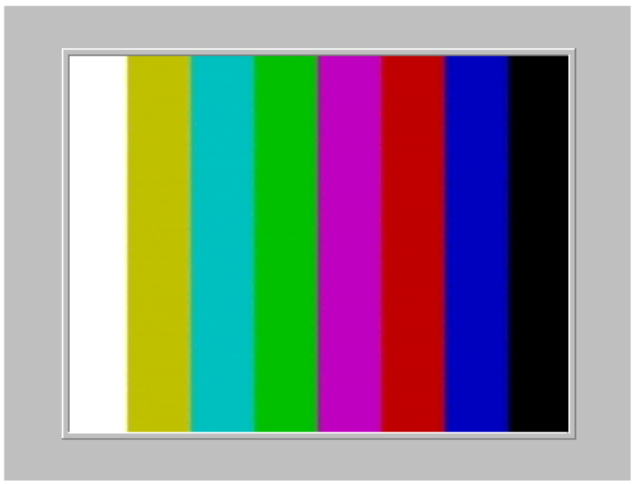
More information on MCC's products can be found on their Web Site at http://www.mcc-us.com or by calling the company directly at (609) 466-1751(New Jersey).

Figure 4. MIIC-201 iPort

Enabling Color Bars

With the hardware and software for ***Bt868 COCKPIT*** in place, the next step is to enable color bars. To enable 100% amplitude and 75% saturation color bars, as shown in Figure 5, do the following:

Figure 5. Color Bars



1. Install the Bt868 ISA card with the Graphics Exxtreme PCI card based on the Permedia2 graphics controller.
2. Turn on the PC.
3. Connect the S-Video or Composite video output from the Bt868EVK to the appropriate external video input of the TV monitor. Switch the TV to view the external video input.
4. In the "Auto Config" subsection of the ***Bt868 COCKPIT*** application, click on the "Default Modes/Mode 0: 640X480, NTSC, RGB" box. This initiates an I^2C write to register 0xB8 of the Bt868 or Bt869.

NOTE: Writing 000 to the Bt868's CONFIG[2:0] bits will launch Auto-Configuration Mode 0. This single byte write automatically loads the 36 values listed in Table 1-5 of the *Bt868/869 Datasheet* to the appropriate Bt868 I^2C registers. The last written values to all of the Bt868's registers can be checked at any time by single clicking on the "Registers" subsection within the ***Bt868 COCKPIT*** application. These registers are all write-only with the exception of the lone read register (see Section 2.3 of the *Bt868/869 Datasheet*). The 36 hex numbers driven by auto-configuration command 0 prompts the Rockwell device to accept a 640X480 resolution, RGB digital input from a graphics controller, and output an NTSC analog video signal. Seven (7) other Auto-Configuration Modes are also possible for various RGB and YCrCb digital inputs. Enabling Auto-Configuration Mode 3 is discussed in the section titled "Displaying 800X600 Mode with the Bt868/869 VGA Encoder" on page 23. Not all I^2C registers are written to after an auto-configuration command.

5. Enable the Bt868's internal color bars by clicking on the "ECBAR" box in the "Input Control" subsection of the ***COCKPIT*** application and then clicking on "Write" in the lower portion of the GUI. This action begins a single byte I^2C write that sets bit 2 of register 0xC4 (ECBAR). This causes the VGA Encoder to ignore any digital data on its input lines and display eight color bars.

6. End the sequence by checking the TV display itself. Step 5 should have enabled all of the analog outputs of the Bt868 to show the eight color bars on the NTSC TV monitor.

NOTE: By default the internal bar colors are fixed in position, hue, brightness, and saturation values. The colors seen should closely resemble the bars shown in Figure 5 (in color if viewing a *.pdf version of this document).

ANY DEVIATION FROM THIS SEQUENCE MIGHT NOT ALLOW COLOR BARS TO BE DISPLAYED. The internal bar color values are actually optimized for YCrCb digital values (Auto-Configuration Modes 5-8) but the quality should be good with RGB values as well.

At this point, if the designer does not observe color bars, then check the I^2C transactions coming from the graphics controller. Also, verify that the ***Bt868 COCKPIT*** program or the graphics controller's write routines are executing properly. If the MIIC-201 adapter and ***Bt868 COCKPIT*** are being used, then there could be an installation problem. Do not install the software contained on the diskette from MCC. Also, the power adapter should not be used, as power is supplied by the Bt868EVK.

If still nothing is seen on the TV, call your local Rockwell Field Applications Engineer.

Displaying 640X480 Mode with the Bt868/869

After correctly displaying color bars, the designer's next step is to implement the 640X480 digital input mode and NTSC TV Out with the Bt868 and the graphics controller.

To easily configure the Bt868 in a mode suitable to handle a 640 active pixel/line X 480 active lines/frame (or 784 total pixels/line X 600 total lines/frame as defined by the Bt868's H_CLKI and V_LINESI registers) RGB digital input, the user should initiate a 1-byte I^2C write for Auto-configuration Mode 0. To do this, the I^2C master should write 000 to the CONFIG[2:0] bits of the 0xB8 register or use the ***Bt868 COCKPIT*** application and click on the Mode 0: 640X480, NTSC, RGB box in the Auto-Configuration subsection. Make sure the EN_OUT bit is set. This bit's address is the LSB (bit 0) of the 0xC4 register. If EN_OUT = 1, then the Bt868 is configured so all outputs are turned on instead of tri-stated.

For graphics controllers which transmit YCrCb pixel data to the Bt868, then Auto-Configuration Mode 4 should be used to program the encoder's I^2C registers appropriately. In either case, after an auto-configuration write, the Bt868 Encoder is ready to receive display data in the chosen format from the graphics controller.

With the Bt868 configured properly, the graphics controller's video output timing registers need to be adjusted accordingly. Specifically, the graphics controller needs to transmit 640 by 480 pixels of active data into the Bt868 at a specific data rate (denoted by CLKI/CLKO) via the Pixel (P0-P23) ports between the two devices.

Auto-Configuration Mode 0, 24-Bit Multiplexed Or Non-Multiplexed RGB Input, Master Interface Mode

The default value for H_CLKO is 1792 (decimal). This means that 1792 clocks per video line are output by the Bt868's clock output (CLKO) and the VGA Encoder expects 1792 clocks per video line to be returned via the clock input (CLKI) from the graphics controller. In other words, 1792 clocks are required to completely encode a full line's worth of data from the Bt868's output.

Since one NTSC line is nominally 63.55556 µs long, the clock rate (or, pixel rate, because data for one pixel is transmitted every clock cycle) is:

$$\frac{1792 \text{ clocks}}{\text{line}} \times \frac{1 \text{ line}}{63.55556\ \mu s} \times \frac{1000000\ \mu s}{1 \text{ second}} = 28, 195, 802$$

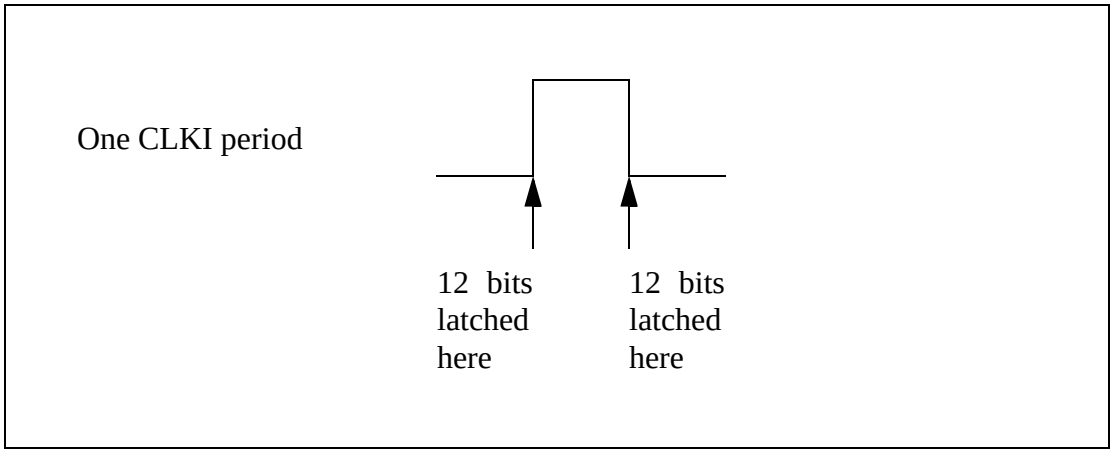
= 28,195,802 clocks/second = **28.195802 MHz**

(The horizontal overscan compensation (HOC) percentage alters this frequency, in this example, HOC = 13.79%. See the section titled "Understanding Overscan Compensation" on page 19.)

If the graphics controller is pixel based, then this means 1 pixel's worth of RGB data or YCrCb data can be transmitted per clock pulse. In this case, the pixel rate equals the clock rate. For 640X480 active display mode, the pixel rate, therefore, needs to be 28.195802 MHz coming from the graphics controller. This frequency will always need to match the frequency coming from the Bt868's CLKO output.

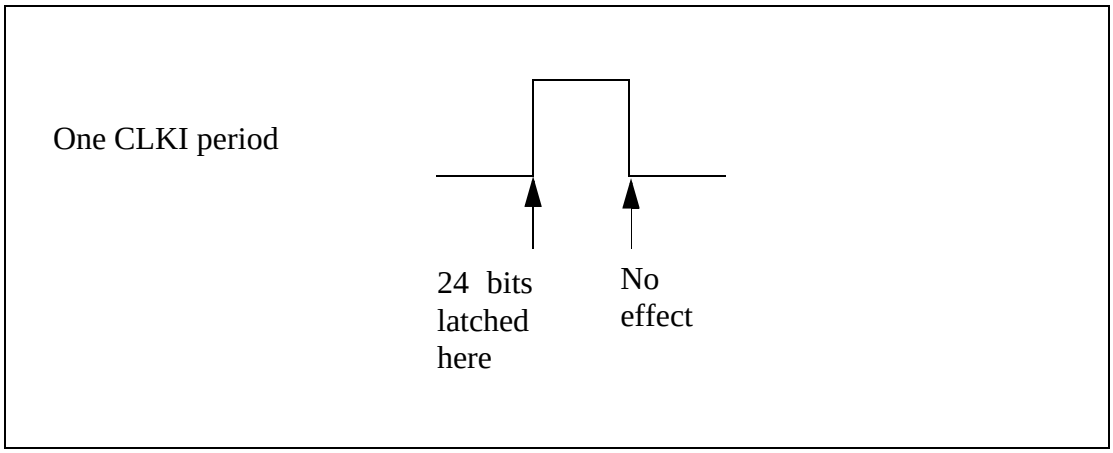
The Bt868 gives a substantial amount of flexibility in how this data is actually sent to the encoder. Either non-multiplexed or multiplexed modes are possible. Multiplexed mode occurs when half of the pixel's data is clocked in on the rising edge of the CLKI signal, and half on the falling edge of CLKI. The result is that one pixel (24 bits of RGB data or 16 bits of YCrCb, etc.) is latched into the encoder on every clock pulse. Refer to Figure 6.

Figure 6. 24-Bit Multiplexed Mode



Non-multiplexed mode exists when each pixel bit has its own dedicated signal line from the graphics controller to the Bt868. 24-bit RGB non-multiplexed mode is shown in Figure 7, where each pixel's worth of data is clocked in on every rising edge of CLKI. The falling edge of CLKI has no effect on the Bt868 itself.

Figure 7. 24-Bit Non-Multiplexed Mode



If the incoming data rate does not equal 28.195802 MHz ± 50 parts per million (ppm) for 640X480, RGB In, NTSC Output mode, the Bt868 does not generate a crisp and/or colored display. In fact, if the tolerance for CLKI varies by more than 50 ppm, color is completely lost. The pixel rate must be adjusted in accordance with the amount of data being sent to the VGA encoder and the video output format being generated. For 800X600 and 640X480 (HOC = 13.79), this frequency needs to be adjusted to the following values:

Input/Output Mode (Default HOC values)	Frequency (MHz)
640X480 Input, NTSC Output	28.195802
800X600 Input, NTSC Output	38.769203
640X480 Input, PAL Output	29.500000
800X600 Input, PAL Output	36.000000

Another method for understanding the frequency calculation is to realize that H_CLKI is equivalent to the number of input pixels per line and V_LINESI is the number of input lines per frame. Multiplying both totals together yields the total number of input pixels per input frame. For Mode 0, 784 x 600 = 470,400 input pixels. Therefore, 59.94005232 fields/second are scanned * (470,400 pixels/field) equals 28,195,802 pixels per second = 28.195802 MHz. Remember that the ratio of graphics controller lines per input frame to encoder lines per output field is the Vertical Scaling Ratio (VSR) and this figure normally ranges from 2.0 – 2.6. Also, one clock is required per pixel (if it is not Mode2X).

The pixel rate is controllable through the use of the graphics controller's 'CRT Timing' registers or 'Video Output Timing' registers. Although the names might vary, the basic registers that need to be programmed in conjunction with the Bt868's registers, are listed below:

- Horizontal Total Register
- Horizontal Display Enable End Register
- Horizontal Blanking Start Register
- Horizontal Blanking End Register
- Horizontal Sync Start Register
- Horizontal Sync End Register
- Vertical Total Register
- Vertical Sync Start Register
- Vertical Sync End Register

- Vertical Display Enable End Register
- Vertical Blanking Start Register
- Vertical Blanking End Register

In master interface mode (most preferred), the Bt868 is the clock timing master, meaning that Rockwell's encoder sends the graphics controller a CLK signal at the proper frequency from our CLKO pin. The graphics controller is expected to take in this signal and send back the pixel data synchronized to that same CLK. The CLK on the CLKI line returned to the Bt868 from the graphics controller is delayed in time from CLKO. If this time delay exceeds 1 clock period, this will cause no problems for the encoder. However, a delay of less than 1 clock cycle should be avoided.

Each pixel input is 2 or 3 bytes in width (depending on whether it is a16-bit or 24-bit input). All of this pixel data is delivered during each CLKI period with the exception of Mode2X (discussed below). For multiplexed modes, half of the data is delivered on the rising edge and half on the falling edge, or all of it on the rising edge in non-multiplexed RGB and YCrCb modes.

Operating the Rockwell device in master interface mode ensures that the accuracy of the clock and video timing signals (HSYNC* and VSYNC*) are derived from the crystal attached to the Bt868's XTALIN and XTALOUT ports. Slave mode subjects the color subcarrier frequency to the tolerance of the graphics controller's crystal and the jitter on the CLKI signal being received by the Bt868.

Depending on the physical interface chosen, the graphics controller's CRT Timing registers need to be set so the horizontal and vertical synchronizing pulses either come from the controller or are received from the encoder. The HSYNC*, VSYNC*, and BLANK* signals are crucial for both devices in determining when the next line starts and ends, and when the next field starts and ends.

For an illustrative analysis of how the Bt868's registers affects the NTSC analog output, please see Figure 10. Because graphics controllers are highly specialized and distinct in register assignments, it is impossible for Rockwell to list individual values to be programmed into each CRT Timing register to send a 640X480 frame. The graphics controller software or BIOS engineer needs to take care of this aspect of his/her own TV Out design.

For cases where a graphics controller does not have the capability to transmit data on both the rising and falling edge of CLKI, then Mode2X for the Bt868/869 must be used. Mode2X is enabled by setting the MODE2X register bit, which is the most significant bit (MSB) of register 0xD4. In this mode, twice the normal CLKI frequency is sent by the graphics controller and half the data is latched by the encoder on the rising edge of the first CLKI cycle and half the data on the rising edge of the second CLKI cycle only. The Bt 868's PLL frequency must also be multiplied by a factor of two for proper Mode2x operation. The encoder will not automatically double its internal frequency, so this step should be handled in software.

Relation of Bt868 Registers to Composite and S-Video Outputs

As mentioned in the section titled "Description of Possible Physical Interfaces" on page 5, the Bt868 outputs composite and S-Video (separate luma and chroma) from the three on-chip digital to analog converters. The analog signal's timing has certain key portions. These regions are the sync, color burst, and active video area. The amount of time for each portion can be controlled with limits via the Bt868's on-chip I^2C registers.

For example, the width of the analog sync pulse can be manipulated via the HSYNC_WIDTH register. For Auto-Configuration Mode 0, the default value is 132 CLKI pulses, which translates to 132*(1/28.195802 MHz) = 4.681µs. This value is listed within NTSC Video Fundamental Specifications and Figure 10. Figure 10 breaks down the effect of various Bt868/869 registers (HBURST_BEGIN, HBURST_END, H_BLANKO, AND H_CLKO) on the analog output being sent to the TV monitor.

Figure 4-2, entitled "Master Mode with Flicker Filter Interface Timing" in the *Bt868/869 Datasheet*, shows the interface signals being sent (HSYNC*, VSYNC*, and BLANK*) to and from the Bt868. Similarly, Figure 4-3 entitled "Slave Mode with Flicker Filter Interface Timing" in the *Bt868/869 Datasheet* shows the necessary timing the graphics controller must meet in slave mode (i.e., HSYNC*, VSYNC*, and BLANK*). Other internal timing parameters are shown in Figures 4-2 and 4-3, but the signals to be scrutinized should be HSYNC*, VSYNC*, and BLANK*. Datasheet Figures 4-2 and 4-3 are reprinted as Figure 8 and Figure 9 in this document.

Figure 8. Master Mode With Flicker Filter Interface Timing

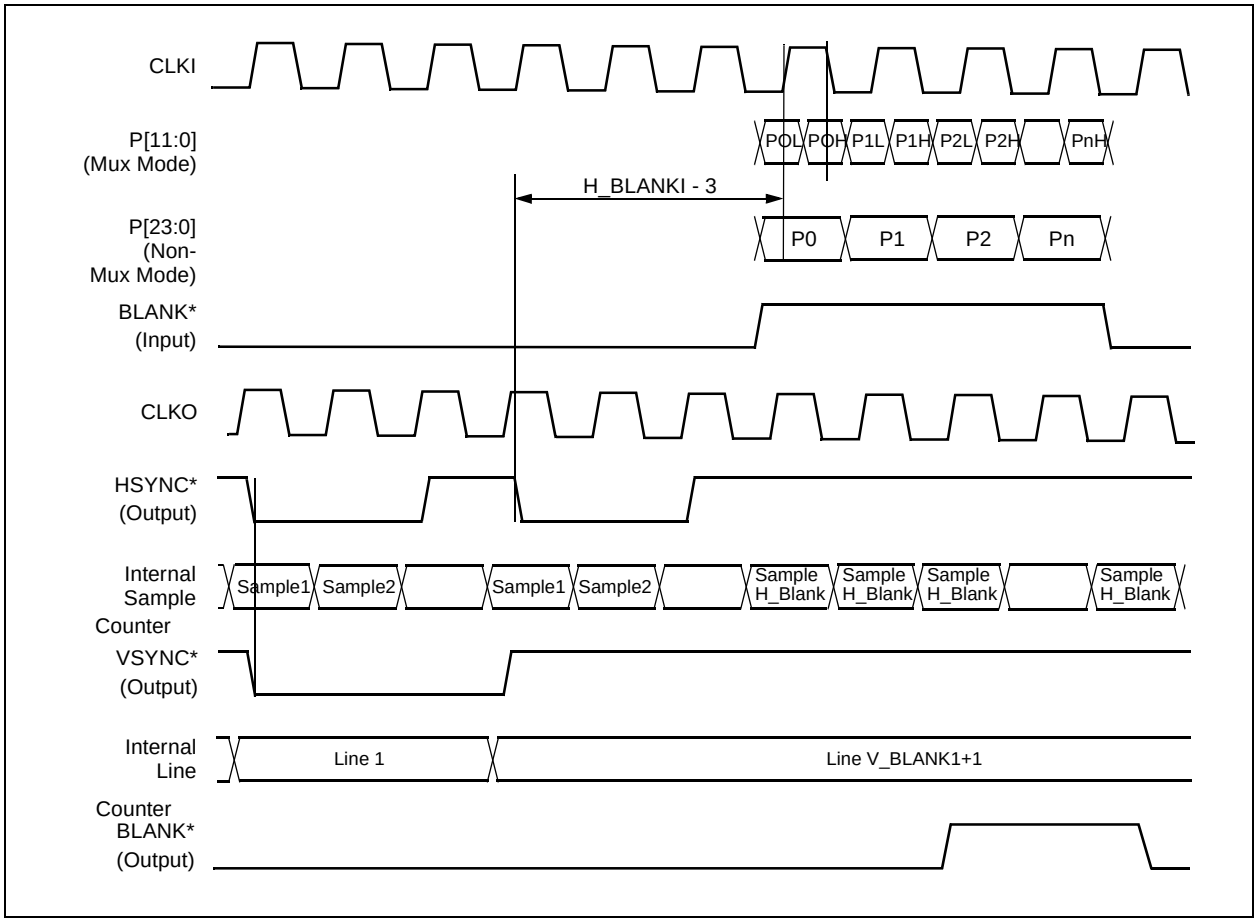
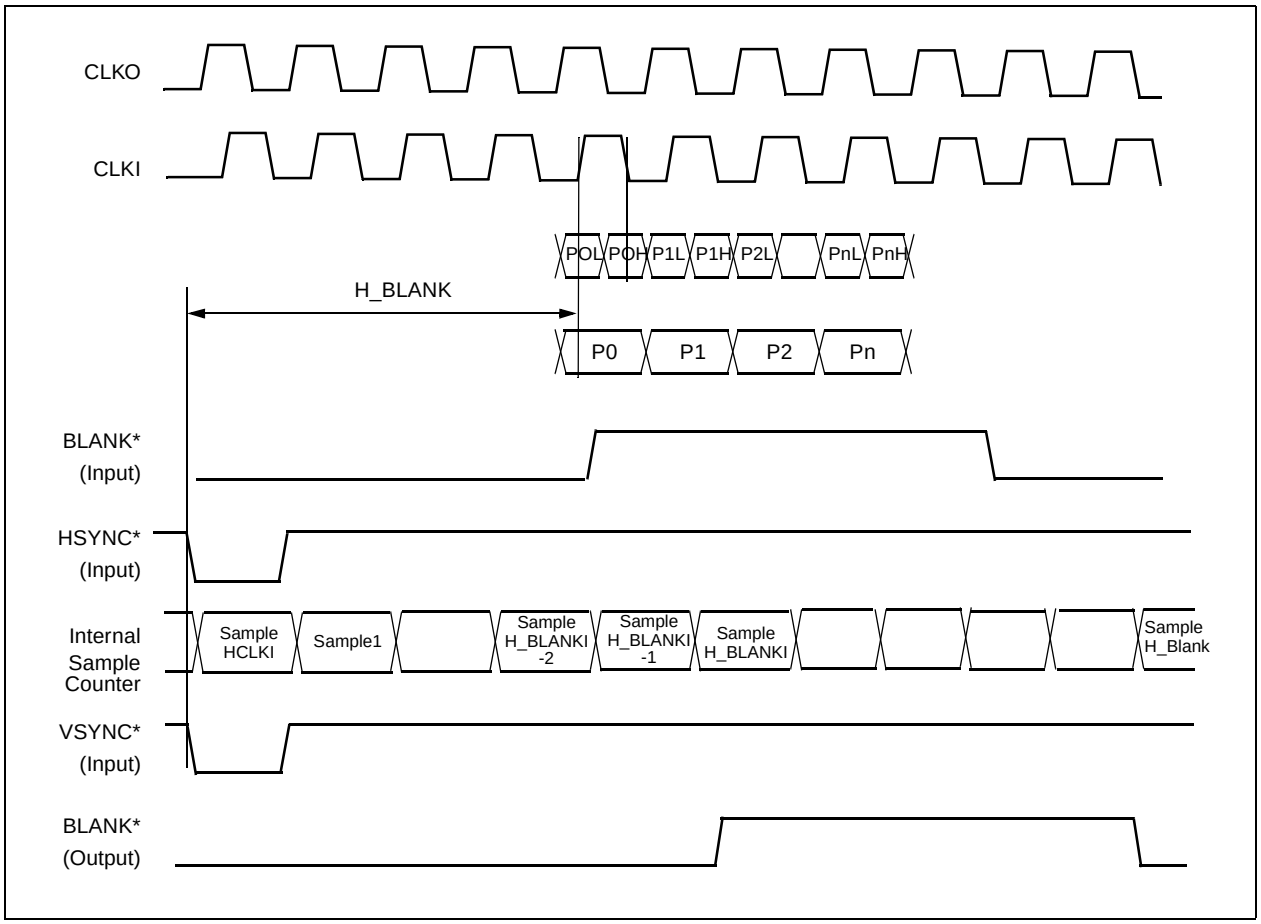


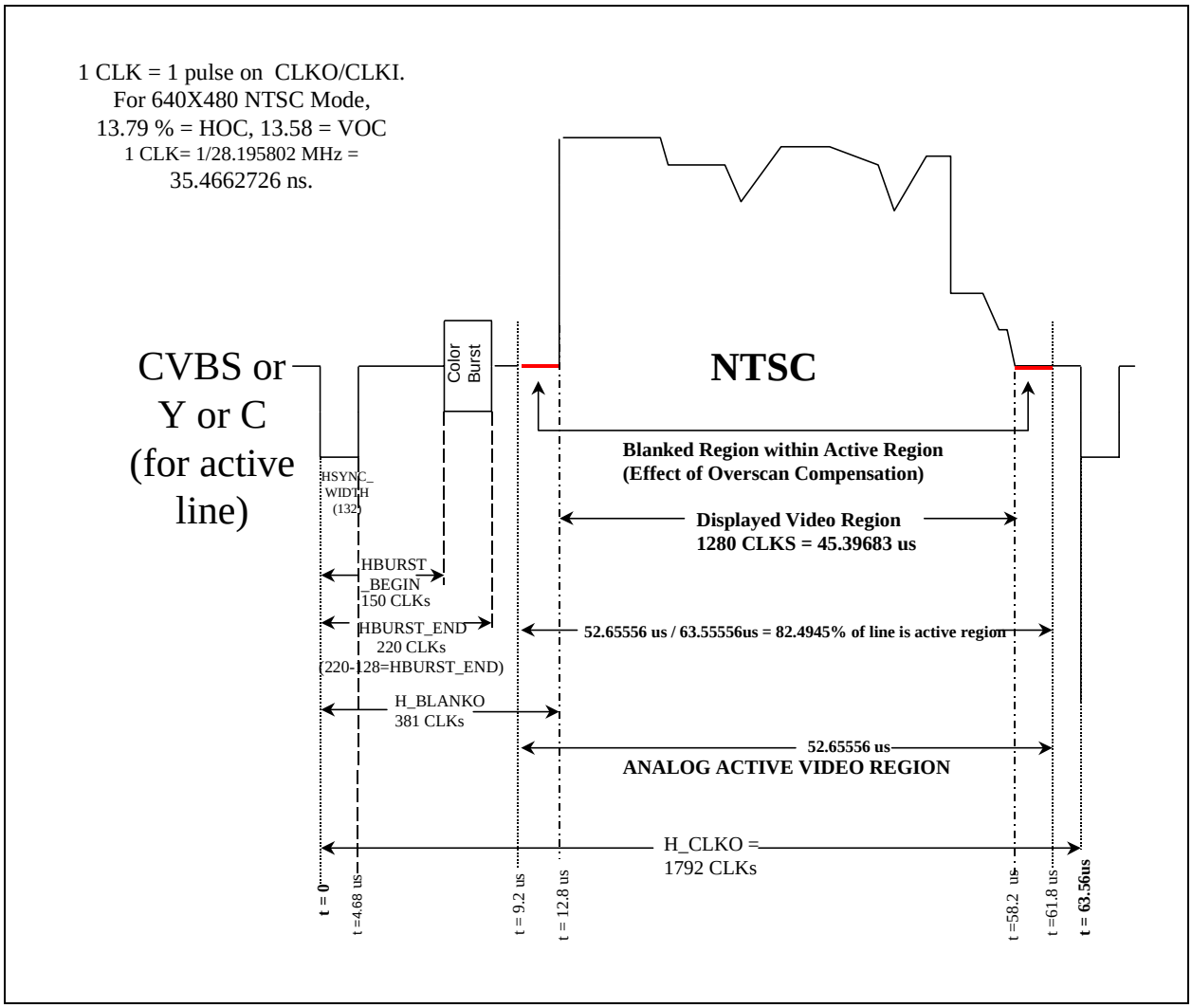
Figure 9. Slave Mode With Flicker Filter Interface Timing



The action of an Auto-Configuration Mode is to set default values into the encoder's most important registers. Figure 10 shows values loaded for Auto-Configuration Mode 0 (640X480 input RGB input, NTSC output) and how they influence the video output from the Bt868/869.

NOTE: A PAL output would look similar to the NTSC illustration.

Figure 10. NTSC Analog Output in Auto-Configuration Mode 0



Understanding Overscan Compensation

One of the Bt868's most interesting and most difficult concepts to grasp is overscan compensation.

As specified in the *Bt868/869 Datasheet* in section 1.3.17, overscan compensation is the process by which the encoder converts "the lines of input pixel data to the appropriate number of output lines for producing a full-screen image on the television receiver." This conversion is done in accordance with the VSR, which is the ratio of number of input lines received to number of output lines generated by the Bt868 (this number is 262.5 lines/field for NTSC). In other words, using the correct amount of compensation in both the horizontal and vertical dimensions ensures that the entire digital image that is normally seen on the PC monitor is satisfactorily mapped to the viewable area of the analog television monitor.

Increasing the HOC percentage while keeping the Vertical Overscan Compensation (VOC) percentage the same has several effects on the VGA Encoder. First, the number of output clocks per line (HCLKO) increases. Correspondingly, the CLKO=CLKI frequency increases. The same 640 active pixels are squeezed into a smaller Display Video Region because the frequency at which input data is clocked into the Bt868 has increased. To compensate for this fact, the graphics controller needs to transmit more blank pixels per line.

Increasing the VOC percentage while keeping the HOC percentage the same has several different effects on the VGA Encoder. First, the HCLKO total stays the same, as does the pixel rate (i.e. CLKI = CLKO). These parameters are dictated by the HOC value. However, the number of total vertical input lines (V_LINESI) increases, which increases the VSR. The net result is that more active pixels and more active lines are used to generate each output line. The only way for the graphics controller to transmit these additional input lines with the same clock frequency as before is to decrease the amount of blanked pixels per line.

The overriding equations for this entire explanation are:

$$\text{VSR} = \frac{\text{V\_LINESI}}{\#\ \text{of total output lines per field}}$$

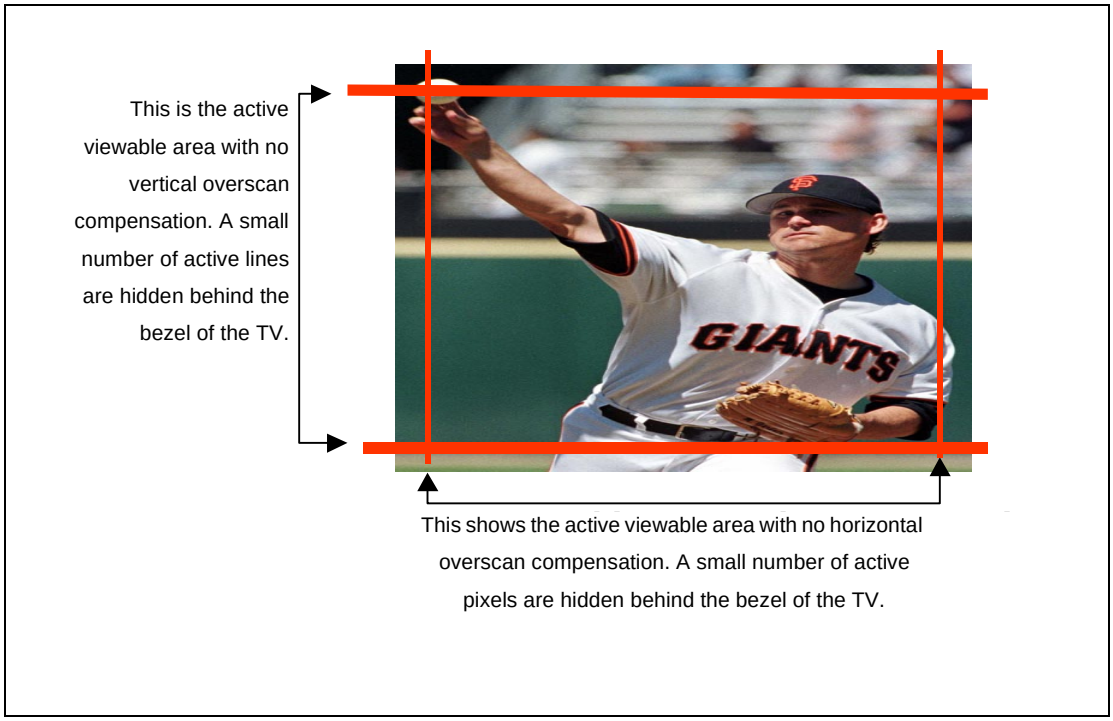
and

$$\#\ \text{blanked pixels} = (\text{H\_CLKO} / \text{VSR}) - \text{H\_ACTIVE}$$

The net result is an interlaced NTSC or PAL video image that fills up the entire TV Monitor. Correct choice of the HOC and VOC percentages guarantees that no regions of the input image are hidden behind the bezel of the TV screen. Various TVs require different HOC and VOC values to fully utilize the entire viewable area of the TV. For the user's convenience, Rockwell has generated Appendix A in the *Bt868/869 Datasheet*, which lists the possible overscan values for the 4 output modes. Varying amounts of blanking are required depending on the HOC, VOC values, and input resolution. The blanked regions are dictated by the BLANK* signal itself and/or the internal pixel counter for the Bt868/869. Actual transmission of null or blanked pixels are not necessary. Only the active pixels need to be sent to the encoder from the controller.

Without overscan compensation, a small percent of the image would be hidden behind the bezel of the TV. See Figure 11 for an illustration.

Figure 11. No Overscan Compensation



Notice a portion of the pitcher's right hand would normally be blocked by the bezel of the TV. This is not normally a problem when watching a sports event or TV show. However, losing the extreme right and left hand sides of the image could pose a serious problem when working with some PC applications. For instance, the **Start** button within the Windows'95 Desktop could be completely hidden from the active viewable region unless compensation was utilized in the horizontal and vertical direction.

To determine what the compensation percentages mean in mathematical terms, the following example is given for 640X480 Mode 0, H_CLKO = 1792, NTSC output, and a 13.785% HOC:

From Table 1-5 of the *Bt868/869 Datasheet*:

# of clocks to latch VSR input lines per analog output line = 1792 CLKs (H_CLKO)

Bt868's 2X upsampling $\geq (2 \times \text{H\_ACTIVE})$ = 1280 active CLKs per analog line

1280/1792 = 71.4286 % of total input data/line used to create 1 line of active video data

a = active region % of analog line = 71.4286 %

b = active region % of typical analog video for NTSC = $\frac{52.65556\ \mu s}{63.55556\ \mu s}$ = 82.4945 % of line is active

$$\text{ratio of a/b} = \frac{71.4286\ \%}{82.4945\ \%} = 0.862147$$

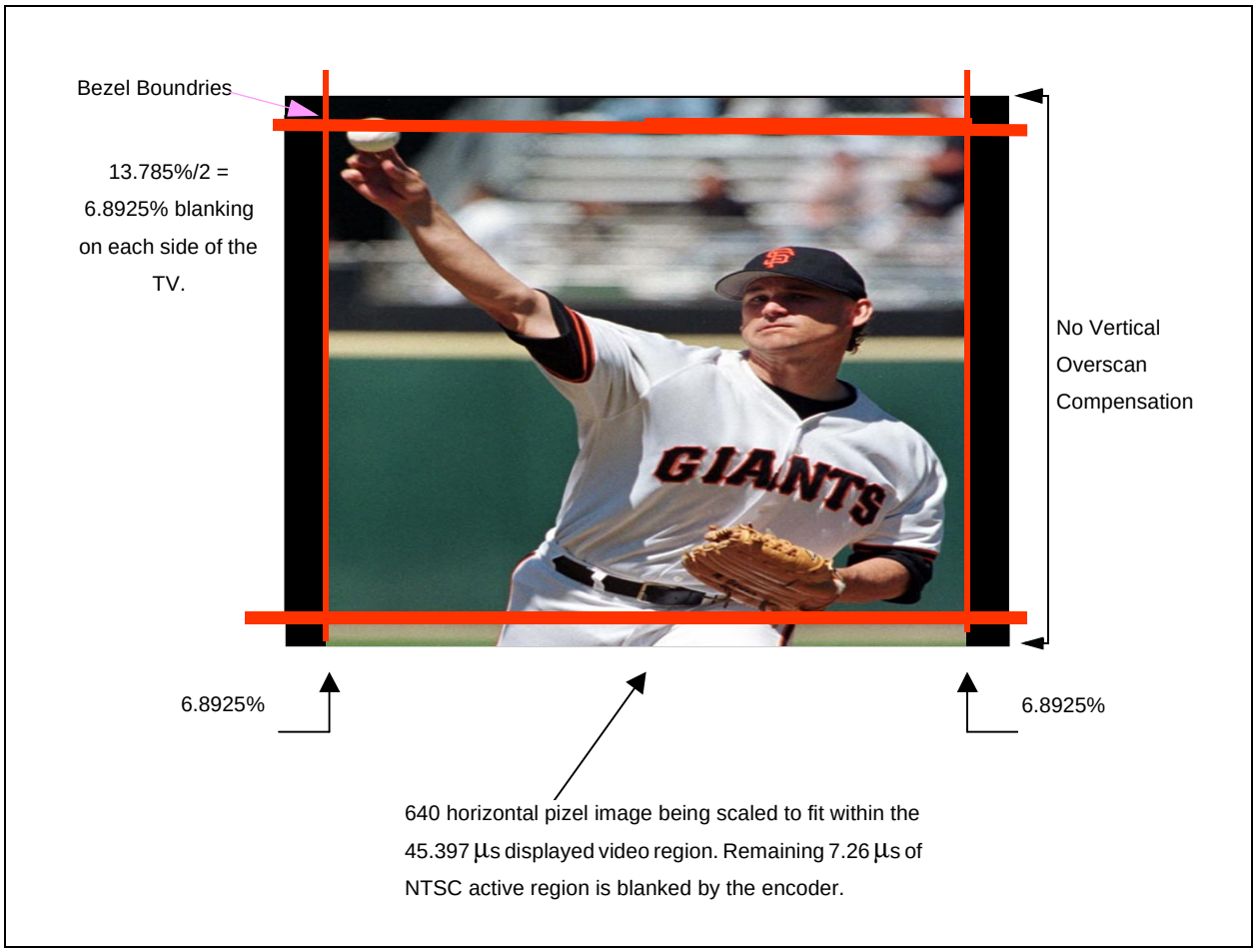
$$1 - 0.862147 = 13.785\ \%$$

This percentage is the HOC value seen in the ***COCKPIT*** application for horizontal overscan compensation. See Figure 12.

Timing Specifics

To resize the upsampled digital image properly for an analog TV monitor, 13.785% HOC is required, which means the Bt868 blanks an extra (13.785% / 2) = 6.89% of the analog region on each side. The original 640 active pixels are squeezed into the remaining analog active region. Furthermore, the Bt868 substitutes blanked pixels in certain portions of the analog line within the active region requiring blanking for overscan compensation.

Figure 12. Horizontally Compensated Image on a TV Monitor



The explanation of the vertical overscan percentage value is similar. For Mode 0, V_ACTIVEO is 212, which means there are 210 full active lines per field. The first and last lines are filtered lines

that assist in smoothing the transitions into and out of the active region to avoid flickering and are not counted. NTSC Video Fundamentals call for 243 active lines per field, so 210/243 = 0.864198 of the vertical active region is used, giving a vertical overscan compensation percentage of 100 - 86.4198 = 13.5802%.

Other Helpful Equations

During 1 encoder output line, VSR (Vertical scaling ratio) total input lines are received. For auto configuration mode 0, the VSR is 2.285714286.

Equation #1: VSR = VLINES_I / # lines in 1 analog output field

= 600 / 262.5 = 2.285714286

Equation #2: The number of clocks per input line can be determined by…

H_CLKI = H_CLKO / VSR

or

1792 / 2.285714286 = 784

NOTE: Flicker filtering and vertical and horizontal overscan compensation are NOT ENABLED in interlaced input mode to the Bt868. Interlaced mode is used for DVD Out from the encoder. Because of the data/image content, flicker filtering and overscan compensation are not necessary in this case.

To interface to the Bt868/869 properly, in order of priority, graphics controllers need to support:

- a non-interlaced data output synchronized with a clock
- possess the ability to accept CLKO for master or pseudo-master mode
- be able to accept HSYNC* and VSYNC* for pure-master or transmit these same signals to the Bt868/869 for pseudo-master or slave modes
- transmit or receive a BLANK* signal

Displaying 800X600 Mode with the Bt868/869 VGA Encoder

After successfully displaying various types of desktop content with 640X480 digital input mode, the designer should attempt to set up an 800X600 input and PAL TV Out with the Bt868 VGA Encoder.

To simply configure the Bt868 in a mode suitable to handle a 800 active pixel/line X 600 active lines/frame (or 960 total pixels X 750 total lines/frame as defined by the Bt868's H_CLKI and V_LINESI registers) RGB digital input and PAL output, the user should initiate a 1-byte I^2C write for Auto-configuration Mode 3. To do this, the graphics controller should write 011 directly to the CONFIG[2:0] bits of the 0xB8 register or use the PC and the ***Bt868 COCKPIT*** and click on the "Default Modes/Mode 3: 800X600, PAL, RGB" box in the "Auto Config" section. Make sure to click on the Enable or Write box as well.

For graphics controllers that transmit YCrCb pixel data to the Bt868, then Auto-Configuration Mode 7 should be used to program the encoder's I^2C registers appropriately. Mode 7 sets up the Bt868 to encode an 800X600 YCrCb digital input into a PAL output. In either case, after a Write command within ***COCKPIT***, the Bt868 Encoder is ready to receive display data from the graphics controller.

With the Bt868 configured properly, the graphics controller's video output timing registers also need to be adjusted accordingly. Specifically, the graphics controller needs to input data into the Bt868 at a specific data rate via the Pixel (P0-P23) ports shared between the two devices.

Auto Configuration Mode 3 = 800X600 RGB input, PAL Output; Master Interface Mode

From the Calculations section, the H_CLKO decimal value is 2304 (900 hex). This means that 2304 clocks per video line are output by the Bt868's clock output (CLKO) and the Bt868 expects 2304 clocks per video line to be returned via its clock input (CLKI).

Since the PAL line is nominally 64.000 µs long, the clock rate (or, pixel rate, because 1 pixel 's data is transmitted each clock pulse) is:

$$\frac{2304 \text{ clocks}}{\text{line}} \times \frac{1 \text{ line}}{64.0000\ \mu s} \times \frac{1000000\ \mu s}{1 \text{ second}} = 36,000,000$$

$$= 36,000,000 \text{ clocks/second} = \mathbf{36.00000\ MHz}$$

If the graphics controller can operate in multiplexed mode (that is, data clocked in on both the rising and falling edge of the CLKI signal), then one pixel (= 16 bits of RGB data) is latched in on every clock pulse. In this case, the pixel rate equals the clock rate. For 800X600 active display mode, the pixel rate needs to be 36.000 MHz ± 25 ppm from the graphics controller.

If the data rate does not equal 36.000 MHz ± 25 ppm for 800X600, RGB In, PAL Out mode, the Bt868 does not generate a non-jittery, crisp, and colored display. The pixel rate and CLKO frequency must be adjusted in accordance with the amount of data being sent to the VGA encoder.

Another method for comprehending this principle is to realize that H_CLKI is equivalent to the number of input pixels per line and V_LINESI is the number of input lines per frame. Multiplying both totals together yields the total number of input pixels per input frame (i.e., per video field). For Mode 3, 960 x 750 = 720,000 input pixels. Therefore, in one second, 50.000 fields are scanned times (720,000 pixels/field) equals 36,000,000 pixels per second = 36.00000 MHz. For 800X600 Auto-Configuration Mode 3, the default HOC value within the Bt868 COCKPIT application is 14.5%. This figure is visible in the Input subsection.

NOTE: Remembering that one controller frame is input per encoder field and that one clock is required per pixel (if it is not Mode2X) helps with these calculations.

To reiterate, the pixel rate is controllable through the use of the graphics controller's 'CRT Timing' registers or 'Video Output Timing' registers. Although the names can vary, the basic registers that need to be programmed are listed in the section titled "Displaying 640X480 Mode with the Bt868/869" on page 13. These registers need to be used for shaping the sync signals, sending the appropriate amount of active data per frame, and enabling blanking when necessary.

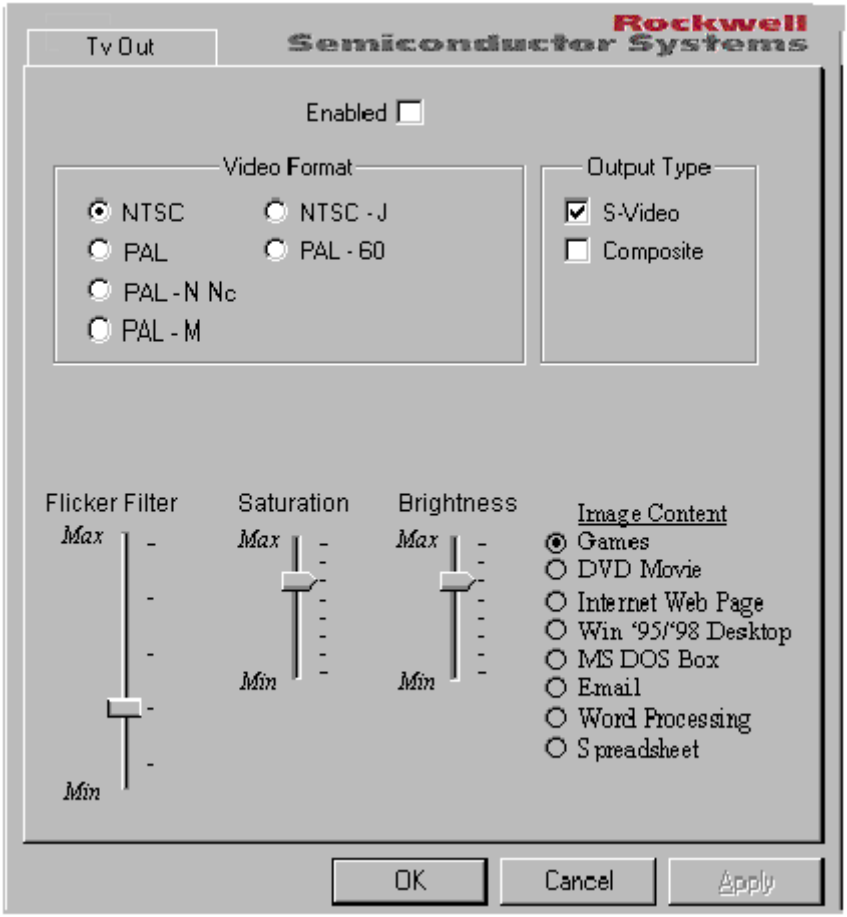
If this has been done and the CRT Timing registers have already been adjusted correctly, and the TV display image is still not stable, then the designer is urged to examine the consistency of the HSYNC* and VSYNC* signals and the BLANK* signal being output to our device by the controller. The HSYNC*, VSYNC*, and BLANK* signals being generated by the controller in pseudo-master and slave modes should be probed with an oscilloscope and analyzed for differences compared to Figure 4-2 and Figure 4-3 in the *Bt868/869 Datasheet*. These diagrams describe in great detail the Master Mode and Slave Mode with flicker filter interface timing. Check if the video timing signals are repeatable and if they exhibit consistent periods.

Sample TV Out Source Code for Graphics Drivers

Although Rockwell provides all the hardware and some software necessary for development of the TV Out solution, we strongly recommend that software engineers skilled in the area of writing graphics drivers work on any project involving the Bt868 or Bt869. To create a suitable production-quality graphics card, new drivers based on C/C++ code must be created that calculate the VGA CRT timing register values based on the Bt868 register values and chosen graphics resolution. The most important equations to drive the Bt868 are already embedded in the source code for the ***Bt868 COCKPIT*** application, but minor modifications and additional code is necessary for a production-quality graphics driver.

Rockwell also urges customers to include more than rudimentary functionality into their GUI interface for TV Out. We suggest a dialog box that looks similar to Figure 13. This type of GUI does not allow the end user the ability to modify every bit or register within the encoder, but does allow him or her the opportunity to enhance the image quality based on content.

Figure 13. Sample GUI Dialog Box



To facilitate this process, Rockwell has generated a spreadsheet for the Bt868/869 that shows optimal internal values for the most popular images seen on a PC. If integrated into actual graphics drivers, these values could reprogram the Bt868 every time the user clicks on the appropriate radio button. This file was created from testing results to determine the most desirable flicker-filter and image settings for the various registers based on the NTSC and PAL video formats. This document is titled "filter_opt_Buteo1.xls" and can be obtained from your local Rockwell Field Applications Engineer. These register values have also been included within a table in the sample source code itself.

To reiterate, this type of GUI does not give the end customer full control over the encoder but it does provide the user an opportunity to optimize the flicker filter configuration for different image types (e.g., games, Web page, spreadsheet).

Although the VGA CRT register addresses are different from controller to controller, their basic functionality remains the same. Taking advantage of this fact, Rockwell has created several generic source code files that should help any graphics controller manufacturer quickly modify the device driver for TV Out.

These files are downloadable via the dedicated Bt868/869 FTP site. For reference, this site's address is: ftp://bt868:tvout@ftp.brooktree.com/

The latest Bt868/869 official layout diagram, ***COCKPIT*** software, product bulletins, and other literature pertinent to Rockwell's VGA encoders also appear on this FTP site.

The sample source code files can all be found in the "app notes" directory and "sample driver source" subdirectory. These files all serve a different purpose and are described briefly below:

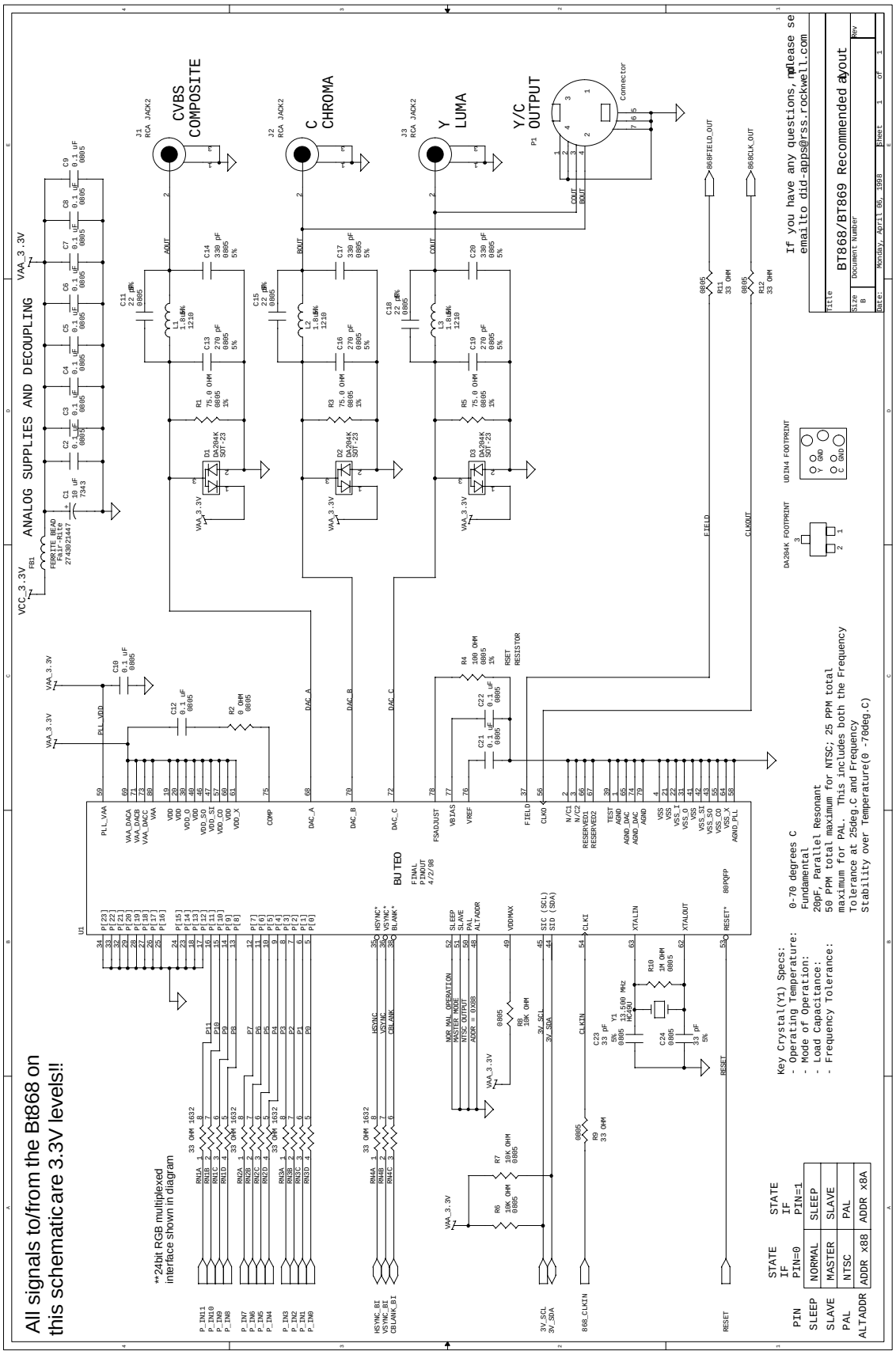
File Name	Purpose
mode_def.h	Declaration/Header file which represents the default register values for each Bt868 or Bt869 auto-configuration mode.
mode_def.cpp	Definition/Implementation file for default register values for each Bt868 or Bt869 auto-configuration mode.
bt868.h	Declaration/Header file of the structures which represent the Bt868 registers and/or individual register bits. Includes I^2C loading function and declaration of optimal filter settings.
bt868.cpp	Definition/Implementation of the structures which represent the Bt868 registers and/or individual register bits. Includes function which implements optimal filter settings.
i2c_skel.def	Module definition file for generic XI2C.dll device driver.
i2c_skel.cpp	Generic skeleton implementation of an XI2C.dll. The graphics controller vendor is still required to modify code so I^2C calls can be made into their graphics adapter driver. Recompilation will be necessary.
main.cpp	Sample implementation of how to program the Bt868 or Bt869. Includes I^2C write routine and load library.

By providing this example source code, Rockwell is attempting to accelerate the design process for all of our potential customers and reduce the time it takes to become familiar with our VGA

encoder's features. In addition to this application note, direct technical assistance can be obtained from your local Rockwell Field Applications Engineer.

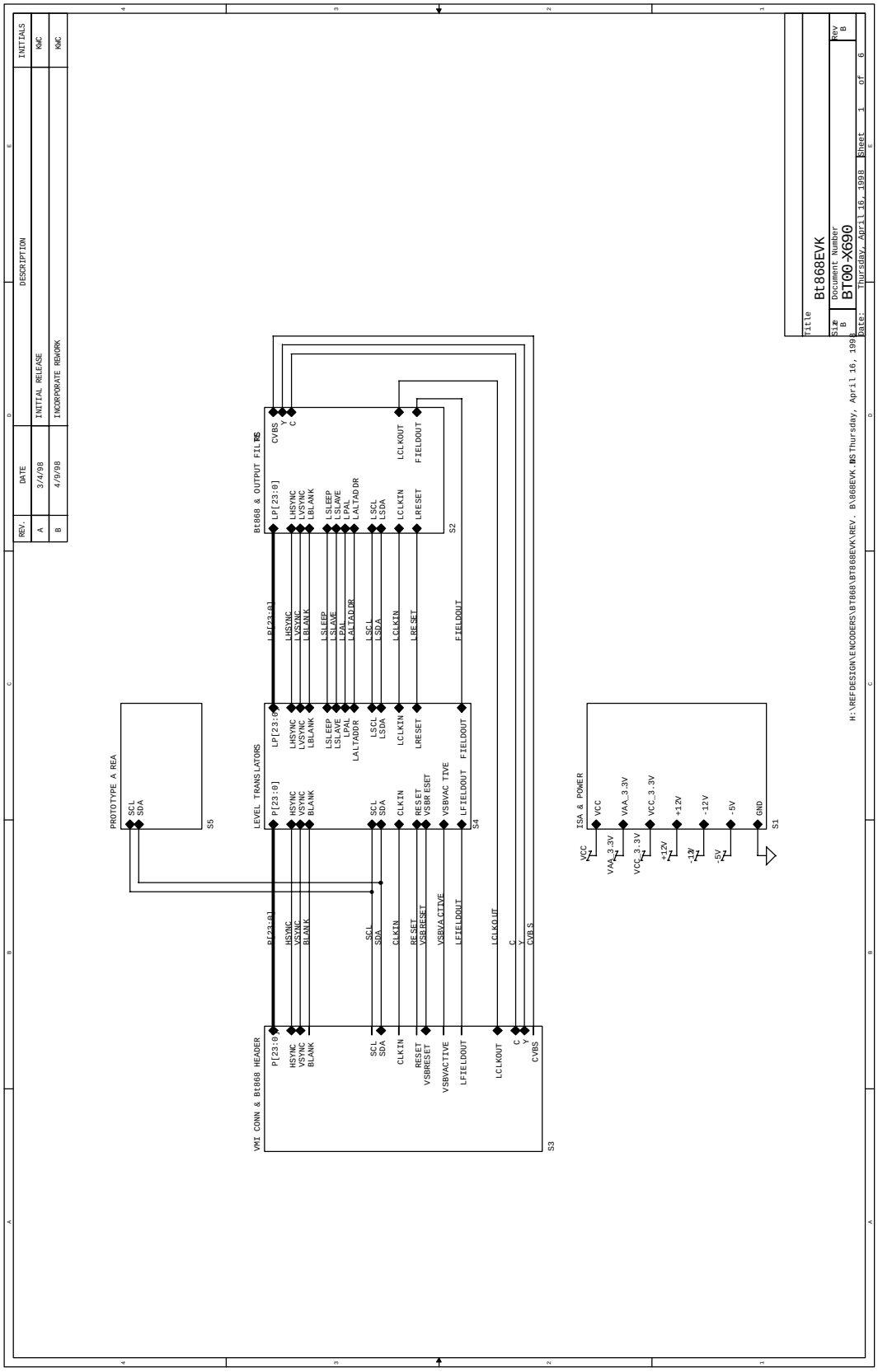
Appendix A Bt868/869 Layout Diagram

The following schematic gives the recommended typical external circuitry for the Bt868/869. The appropriate post D-A converter elliptical low-pass filters have also been included.


All signals to/from the Bt868 on this schematic are 3.3V levels!!
**24bit RGB multiplexed interface shown in diagram
ANALOG SUPPLIES AND DECOUPLING
CVBS COMPOSITE
C CHROMA
Y LUMA
Y/C OUTPUT
BU TEO
Key Crystal(Y1) Specs:
- Operating Temperature: 0-70 degrees C
- Mode of Operation: Fundamental
- Load Capacitance: 20pF, Parallel Resonant
- Frequency Tolerance: 50 PPM total maximum for NTSC; 25 PPM total maximum for PAL. This includes both the Frequency Tolerance at 25deg.C and Frequency Stability over Temperature(0 -70deg.C)
If you have any questions, please se emailto did-apps@rss.rockwell.com
BT868/BT869 Recommended layout
Document Number
Monday, April 06, 1998
PIN STATE IF PIN=0 STATE IF PIN=1
SLEEP NORMAL SLEEP
SLAVE MASTER SLAVE
PAL NTSC PAL
ALTADDR ADDR x88 ADDR x8A

Appendix B Bt868 ISA Card Schematic

The schematic for the Bt868 ISA card is found on the following pages.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A 3/4/98 INITIAL RELEASE MWC
B 4/9/98 INCORPORATE REWORK MWC
Bt868EVK
Document Number
BT00-X690
Rev B
Sheet 1 of 6
Thursday, April 16, 1998
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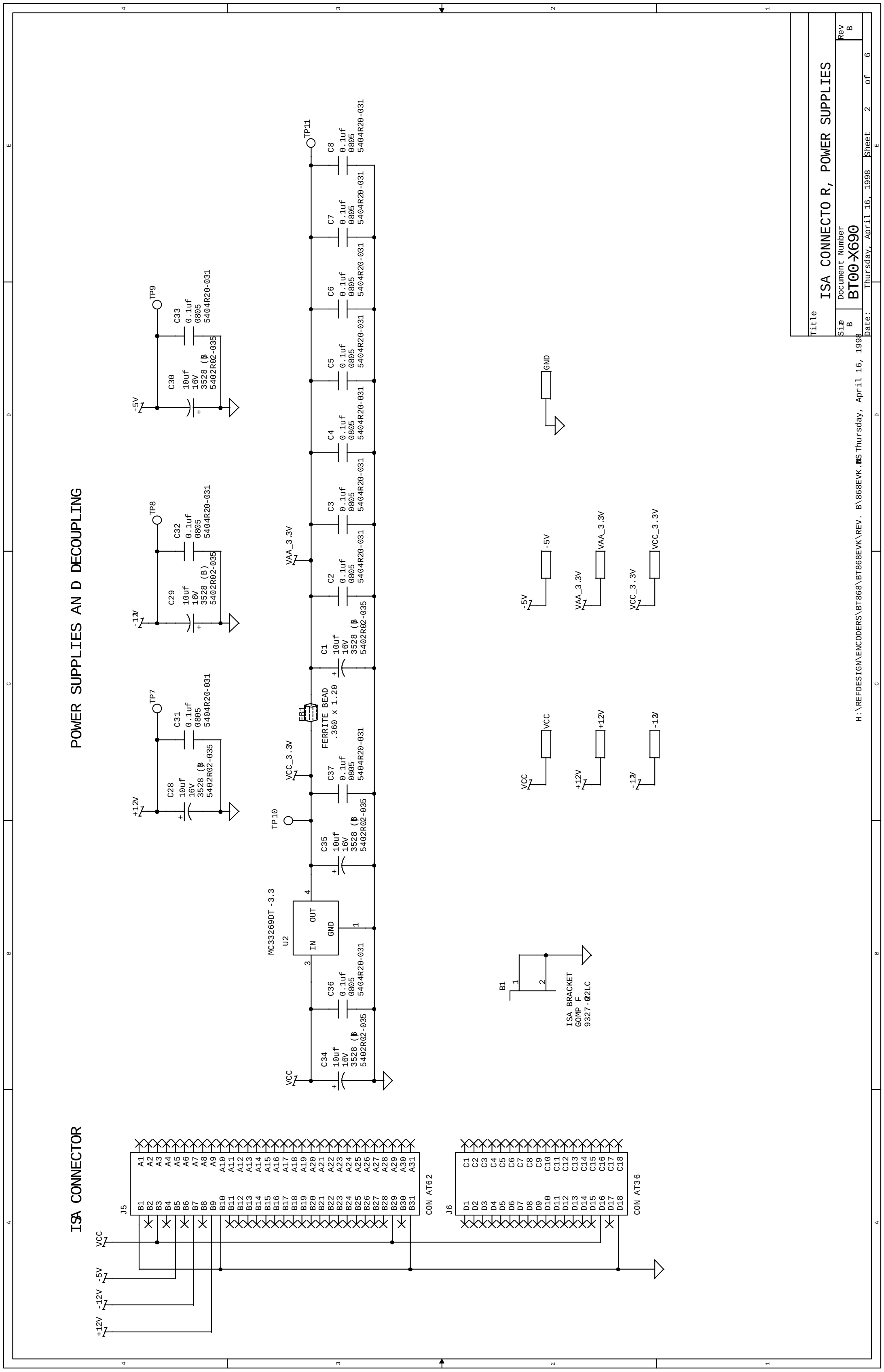
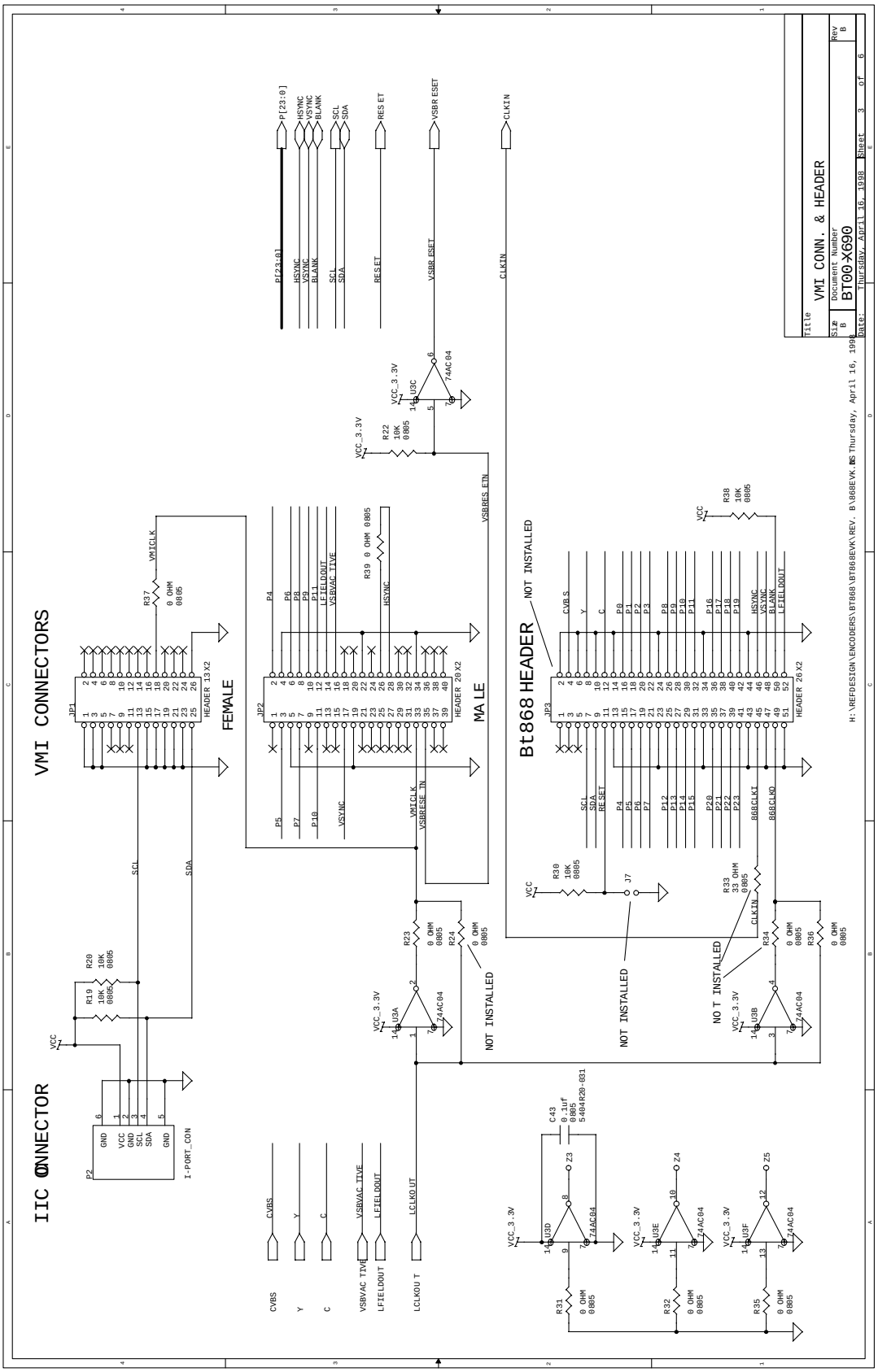
Bt868 & OUTPUT FILTERS
LEVEL TRANSLATORS
VMI CONN & Bt868 HEADER
PROTOTYPE A REA
ISA & POWER
LP[23:0]
HSYNC
VSYNC
BLANK
LSLEEP
LSLAVE
LPAL
LALTADDR
LSCL
LSDA
LCLKIN
LRESET
FIELDOUT
CVBS
C
Y
LCLKOUT
P[23:0]
RESET
VSBRESET
VSBVACTIVE
LFIELDOUT
SCL
SDA
CLKIN
VCC
VAA_3.3V
VCC_3.3V
+12V
-12V
-5V
GND
S1
S2
S3
S4
S5


POWER SUPPLIES AND DECOUPLING
ISA CONNECTOR
ISA CONNECTOR, POWER SUPPLIES
BT00-X690
Thursday, April 16, 1998
Sheet 2 of 6


VMI CONNECTORS
IIC CONNECTOR
FEMALE
MALE
Bt868 HEADER
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NOT INSTALLED
NOT INSTALLED
NOT INSTALLED
I-PORT_CON
HEADER 13X2
HEADER 20X2
HEADER 26X2
74AC04
P[23:0]
HSYNC
VSYNC
BLANK
SCL
SDA
RESET
VSBR ESET
CLKIN
VSBRES_IN
VMICLK
LFIELDOUT
VSBVAC_TIVE
LCLKOUT
CVBS
Y
C
VCC
VCC_3.3V
R37 0 OHM 0805
R39 0 OHM 0805
R38 10K 0805
R30 10K 0805
R33 33 OHM 0805
R22 10K 0805
R19 10K 0805
R20 10K 0805
R23 0 OHM 0805
R24 0 OHM 0805
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Title VMI CONN. & HEADER
Size B
Document Number BT00-X690
Rev B
Date: Thursday, April 16, 1998
Sheet 3 of 6
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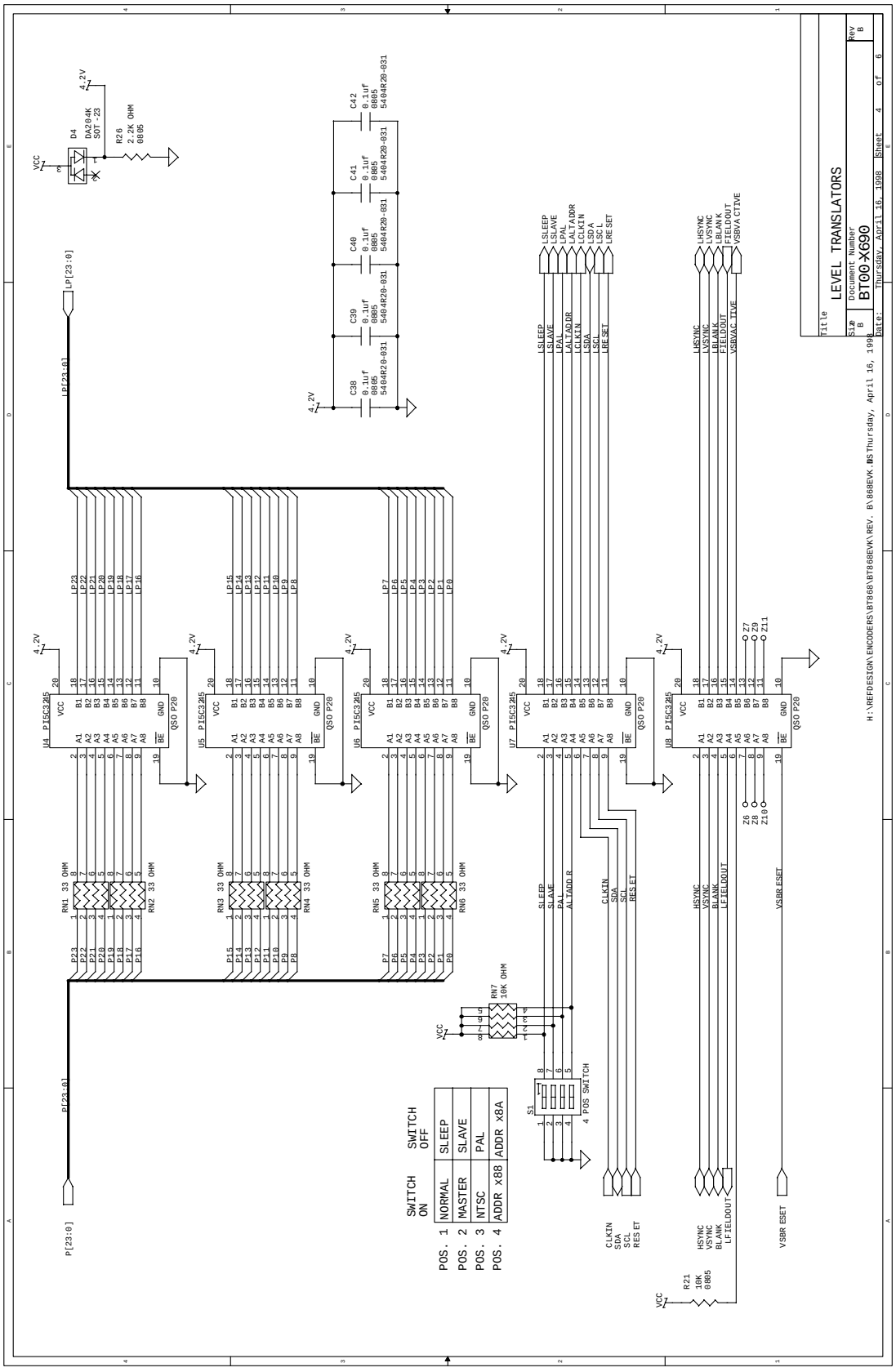
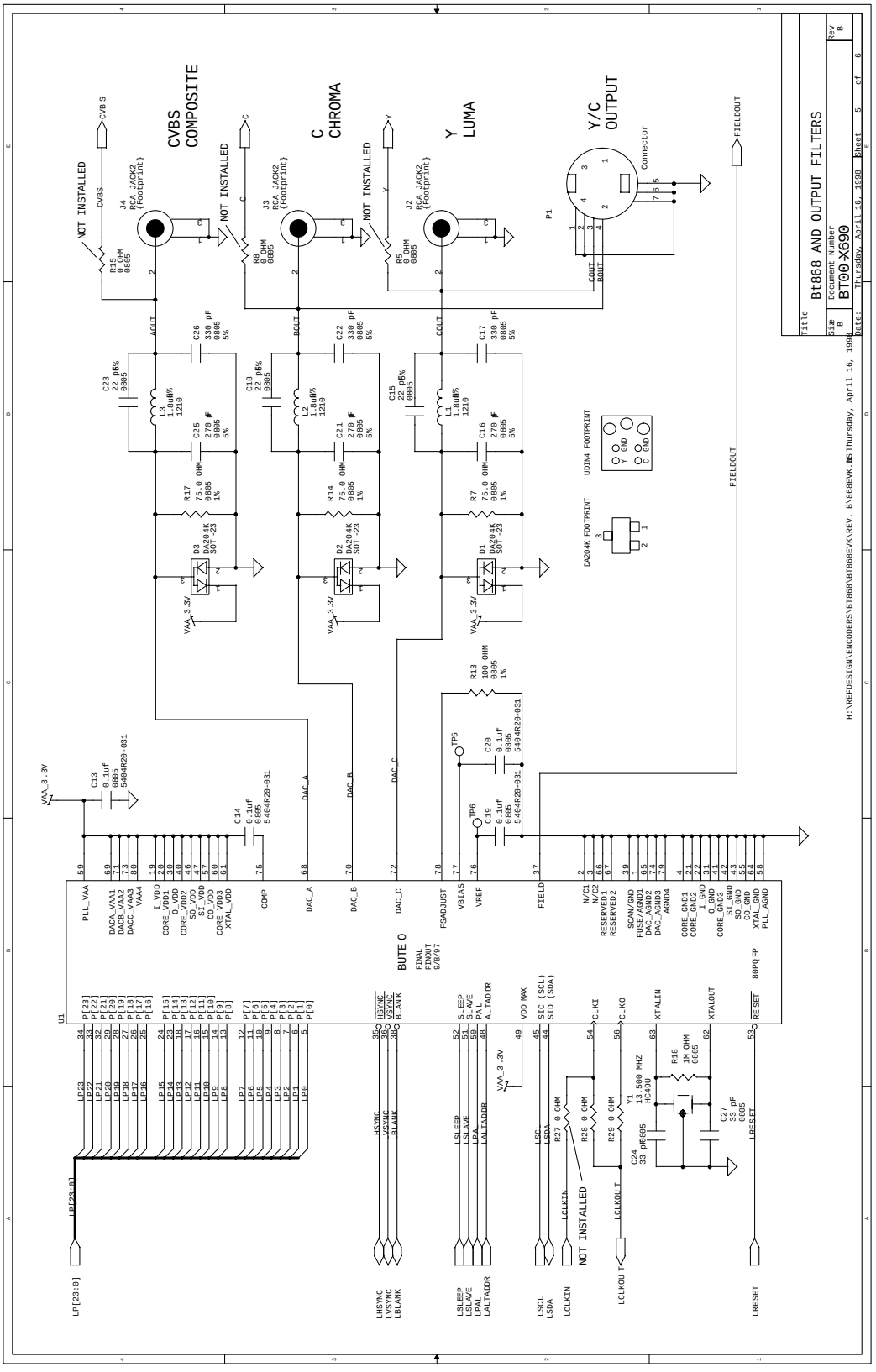

LEVEL TRANSLATORS
Document Number
BT00-X690
Rev B
Sheet 4 of 6
Thursday, April 16, 1998
H:\REFDESIGN\ENCODERS\BT868\BT868EVK\REV. B\868EVK.DSThursday, April 16, 1998
SWITCH ON
SWITCH OFF
POS. 1 NORMAL SLEEP
POS. 2 MASTER SLAVE
POS. 3 NTSC PAL
POS. 4 ADDR x88 ADDR x8A
4 POS SWITCH
VSBR ESET
CLKIN
SDA
SCL
RES ET
HSYNC
VSYNC
BLANK
FIELDOUT
VSBVA CTIVE
LSLEEP
LSLAVE
LPAL
LALTADDR
LCLKIN
LSDA
LSCL
LRESET


CVBS
COMPOSITE
C
CHROMA
Y
LUMA
Y/C
OUTPUT
NOT INSTALLED
J4
RCA JACK2
(Footprint)
J3
RCA JACK2
(Footprint)
J2
RCA JACK2
(Footprint)
P1
Connector
U1
BT868 AND OUTPUT FILTERS
Document Number
BT00-X690
Rev
B
Sheet 5 of 6
Thursday, April 16, 1998
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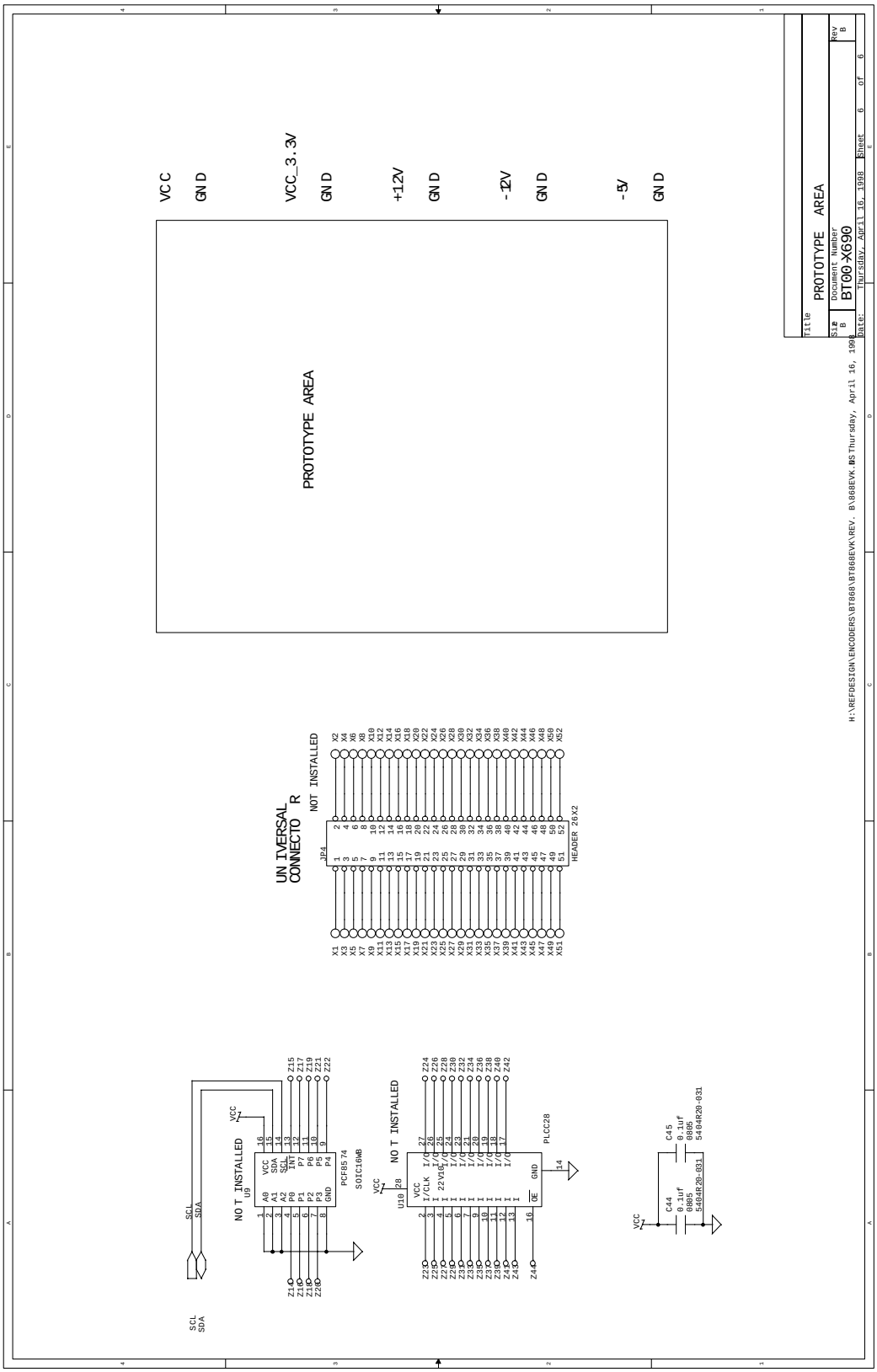
LP[23:0]
LHSYNC
LVSYNC
LBLANK
LSLEEP
LSLAVE
LPAL
LALTADDR
LSCL
LSDA
LCLKIN
LCLKOUT
LRESET
FIELDOUT
VAA_3.3V
DA204K FOOTPRINT
UDIN4 FOOTPRINT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GND
VCC_3.3V
GND
+12V
GND
-12V
GND
-5V
GND
PROTOTYPE AREA
PROTOTYPE AREA
Title
Size B
Document Number
BT00-X690
Rev B
Date: Thursday, April 16, 1998
Sheet 6 of 6
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JP4
HEADER 26X2
NOT INSTALLED
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PCF8574
SOIC16WB
NOT INSTALLED
U10
PLCC28
C44
0.1uf
0805
5404R29-031
C45
0.1uf
0805
5404R29-031
SCL
SDA

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WORLDWIDE HEADQUARTERS

Rockwell Semiconductor Systems
4311 Jamboree Road
P.O. Box C
Newport Beach, CA
92658-8902

Phone: (949) 221-4600
Fax: (949) 221-6375

AMERICAS

US Northwest/Pacific Northwest
Phone: (408) 249-9696
Fax: (408) 249-7113

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Fax: (281) 955-2913

US Northeast
Phone: (978) 692-7660
Fax: (978) 692-8185

US Southeast
Phone: (770) 246-8283
Fax: (770) 246-0018

Phone: (919) 786-4002
Fax: (919) 782-8727

US Florida
Phone: (727) 799-8406
Fax: (727) 799-8306

South America
Phone: 55 11 3874 8978
Fax: 55 11 3874 8883

US Mid-Atlantic
Phone: (215) 244-6784
Fax: (215) 244-9292

EUROPE

European Headquarters
Rockwell Semiconductor Systems S.A.S
Les Taissounieres B1
1680 Route des Dolines
BP 283
06905 Sophia Antipolis Cedex, France
Phone: (33-4) 93 00 33 35
Fax: (33-4) 93 00 33 03

Europe Central
Phone: (49-89) 829-1320
Fax: (49-89) 834-2734

Europe Mediterranean (Satellite)
RSS
c/o Rockwell Automation S.r.l.
Phone: (34-91) 565 16 16
Fax: (34-91) 565 16 87

Europe Mediterranean
Phone: (39-2) 93179911
Fax: (39-2) 93179913

Europe North
Phone: (44-1344) 486 444
Fax: (44-1344) 486 555

Europe South
Phone: (33-1) 49 06 39 80
Fax: (33-1) 49 06 39 90

Europe Israel
Phone: (972-9) 9524 000
Fax: (972-9) 9573 732

APAC

APAC Headquarters
Rockwell Int'l Manufacturing Pte Ltd.
1 Kim Seng Promenade
#09-01 East Tower
Great World City
Singapore 237994
Phone: (65) 737-7355
Fax: (65) 737-9077

Australia
Phone: (61-2) 9869 4088
Fax: (61-2) 9869 4077

China
Phone: (86-21) 6361-2515
Fax: (86-21) 6361-2516

Europe North (Satellite)
Phone: (46) 8 477 4036
Fax: (46) 8 477 4037

TAIWAN

Taiwan Headquarters
Rockwell Int'l Taiwan Company, Ltd.
Room 2808 International Trade Bldg.
333 Keelung Road, Section I
Taipei, Taiwan
10548 ROC
Phone: (886-2) 2-720-0282
Fax: (886-2) 2-757-6760

JAPAN

Japan Headquarters
Rockwell Int'l Japan Co. Ltd.
Shimomoto Bldg.
1-46-3 Hatsudai, Shibuya-ku
Tokyo, 151 Japan
Phone: (81-3) 5371 1520
Fax: (81-3) 5371 1501

Hong Kong
Phone: (852) 2 827-0181
Fax: (852) 2 827-6488

India
Phone: (91-11) 692-4780
Fax: (91-11) 692-4712

Korea
Phone: (82-2) 565-2880
Fax: (82-2) 565-1440