OV511

Advanced Camera to USB Bridge
OmniVision Technologies, Inc.
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Data Sheet ***Rev. 1.0***

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1 Features

- Camera Input: 16-bit YUV 4:2:2/RGB raw data formats (two channels) or 8-bit Y 4:0:0/RGB raw data formats (one channel only)
- Supports clamping, down-scaling & filtering circuits for different video formats (VGA, CIF & QCIF)
- Supports proprietary real-time compression of up to 7:1
- USB camera system: OV511 + 256Kx16 5V EDO, RAS-BEFORE-CAS refresh, 60ns DRAM, + USB transceiver
- Supports hardware & software snapshot functions
- Supports suspend / resume function
- Supports USB running at the setting of full speed signaling bit rate
- Supports USB control and isochronous transfers
- Supports 8 alternates of up to 8Mbps USB transfer rate
- Supports I^2C master function running at 100KHz (normal mode)
- Supports bus powered function of USB standard
- Supports standard interface of USB transceivers
- Optional single/dual clock inputs, hardware selectable

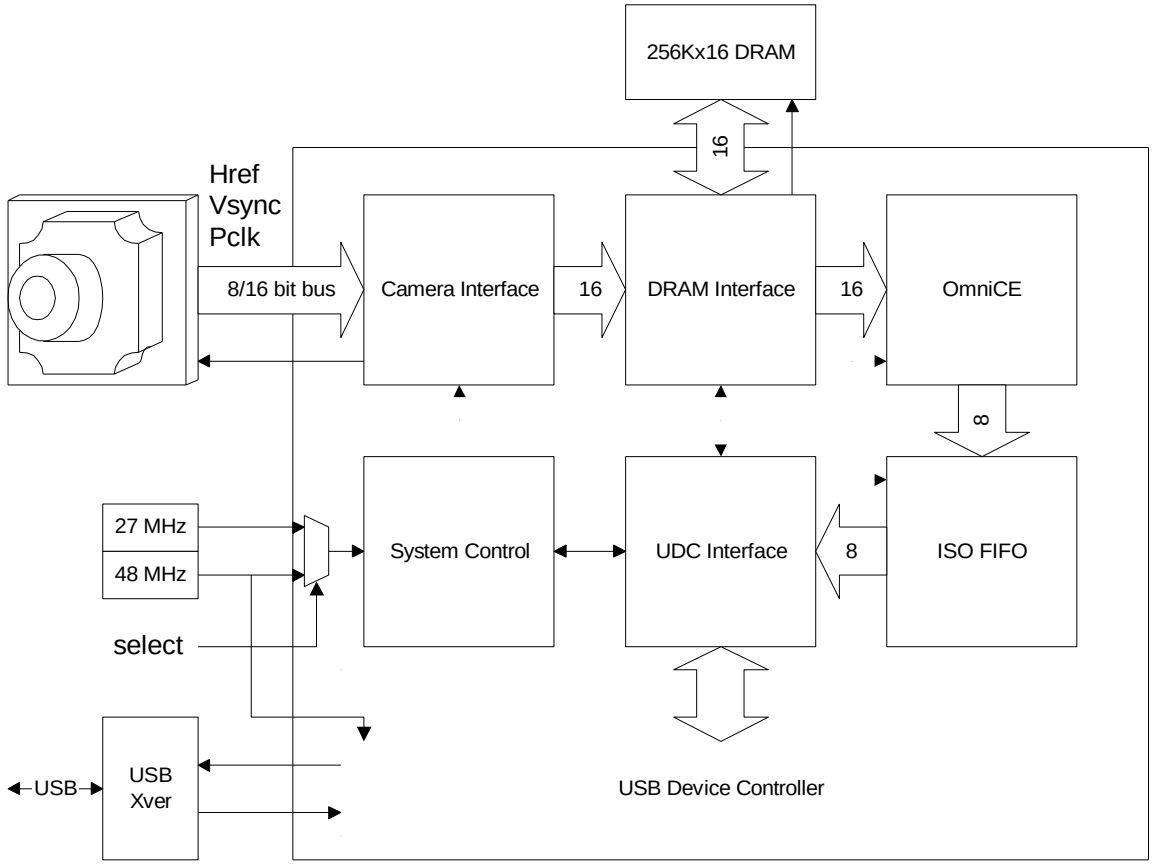
2 Architecture

2.1 General Description

The ***OV511 Advanced Camera to USB Bridge*** is an USB camera controller that includes a compression function which supports real time image transfer and display in the PC system. A complete USB camera system consists of OV511, a 256Kx16 DRAM, an USB transceiver, and a digital camera such as OV7610. The Camera Interface generates different image formats by taking either 16-bit YUV 4:2:2/RGB raw data or 8-bit Y 4:0:0/RGB raw data inputs. The OmniCE is a proprietary compression engine. It not only performs 30fps compression rate for CIF image, but also allows fast decompression in the host. In order to control camera devices, users can choose either I^2C or Parallel IO bus. The I^2C bus master uses two dedicated pins "SDA" & "SCL", while the PIO shares with Y & UV buses. A hardware camera snapshot feature is also implemented in addition to the software snapshot launched by the host. This allows camera to alter formats before taking the shot.

The functional blocks of OV511, as shown in the following figure, consist of Camera Interface, DRAM Interface, OmniCE, UDC interface, ISO FIFO, System Control, I^2C and PIO.

Figure 1. Functional Block Diagram



2.2 Functional Description

2.2.1 Camera Interface

The OV511 digital video inputs are either 16-bit YUV 4:2:2/RGB raw data formats (two channels) or 8-bit Y 4:0:0/RGB raw data formats (one channel only). Clamping, down-scaling & filtering functions are also supported. However, not all input formats can be compressed by OmniCE.

Table 1. Capability of Camera Interface

Channels	Input Formats	Clamping	Down-Scaling	Filtering	Compression (OmniCE)
2, 16-bit (Y & UV)	YUV 4:2:2	Available	Available	Available	Available
	16-bit RGB raw data	Available	Available	Available	Not available
1, 8-bit (Y only)	Y 4:0:0	Available	Available	Available	Available
	8-bit RGB raw data	Available	Available	Not available	Not available

If the camera input format is 16-bit YUV 4:2:2 mode, the output of the camera interface can be configured as YUV 4:2:0 or 4:0:0, as well as YUV 4:2:2.
The maximum clamped image size is 1024 pixels wide and 1024 lines height in increment of 8, depending on the camera input format. The actual image size is limited by the capability of DRAM.

Table 2. Maximum Pixel Count of one 256KX16 DRAM

Output Formats of Camera Interface	Pixel Count
YUV 4:2:2	256K
YUV 4:2:0	344K
Y 4:0:0	512K

The down-scaling feature sub-samples the image in both horizontal & vertical directions by choosing scaling factor 1, 2, 4 or 8. No up-scaling feature is implemented.
The anti aliasing filter interploates down-scaling images to improve image resoultion.
The camera interface can perform capture of one single frame as well as video, such as VGA, CIF or QCIF easily.

Figure 2. Camera Interface YUV - 4:2:2 - 16-bit Horizontal Timing Waveforms

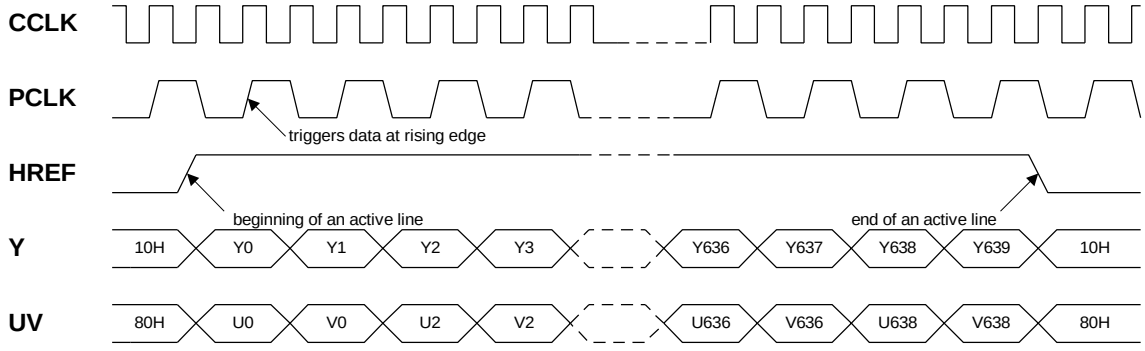


Figure 3. Camera Interface Vertical – Interlace Mode Timing Waveforms

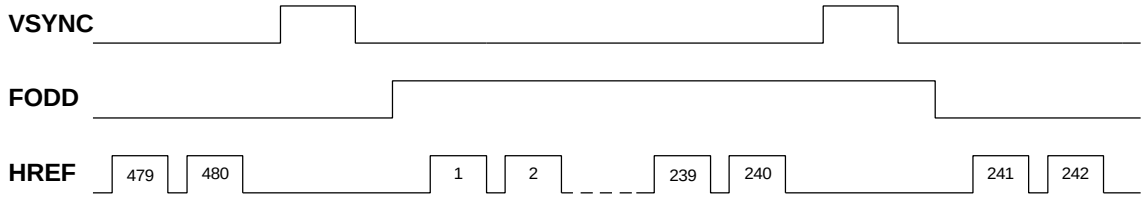
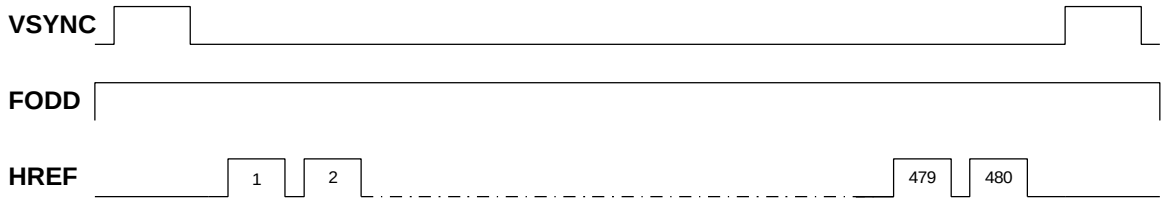


Figure 4. Camera Interface Vertical – Progressive Mode Timing Waveforms



2.2.2 DRAM Interface

DRAM interface generates DRAM addresses for Write and Read cycles based on the configured image size as well as data format. The DRAM memory is partitioned according to the data formats such as 4:2:2, 4:2:0 or 4:0:0.

DRAM interface also arbitrates the DRAM access between write request from the camera interface and read request from OmniCE. It also performs the flow control to avoid image overflow and underflow conditions occur.

OV511 supports 5V EDO, RAS-BEFORE-CAS refresh, 60ns DRAM.

Figure 5. Memory Map

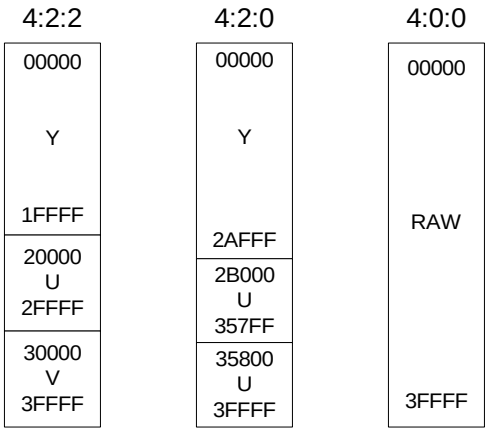


Figure 6. DRAM Interface Write Cycle Timing Waveforms

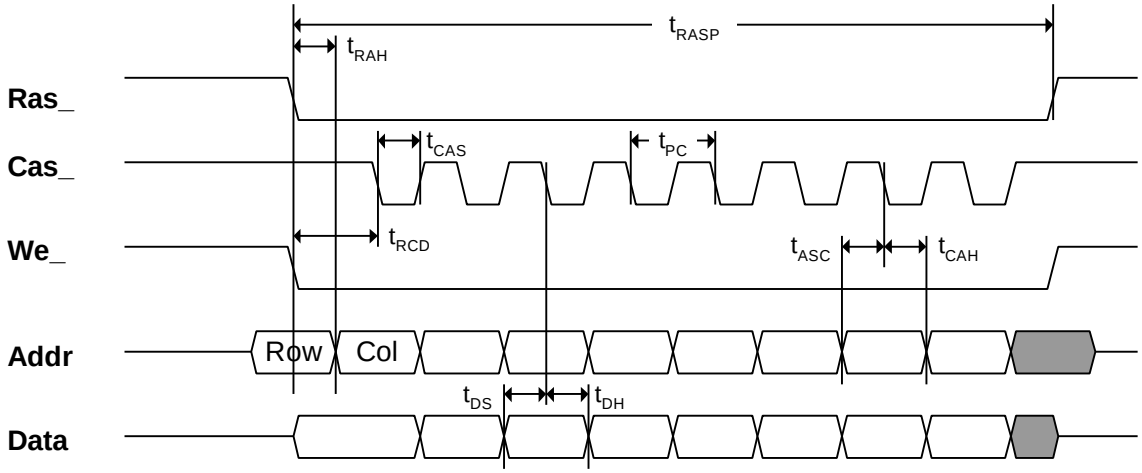


Figure 7. DRAM Interface Read Cycle Timing Waveform

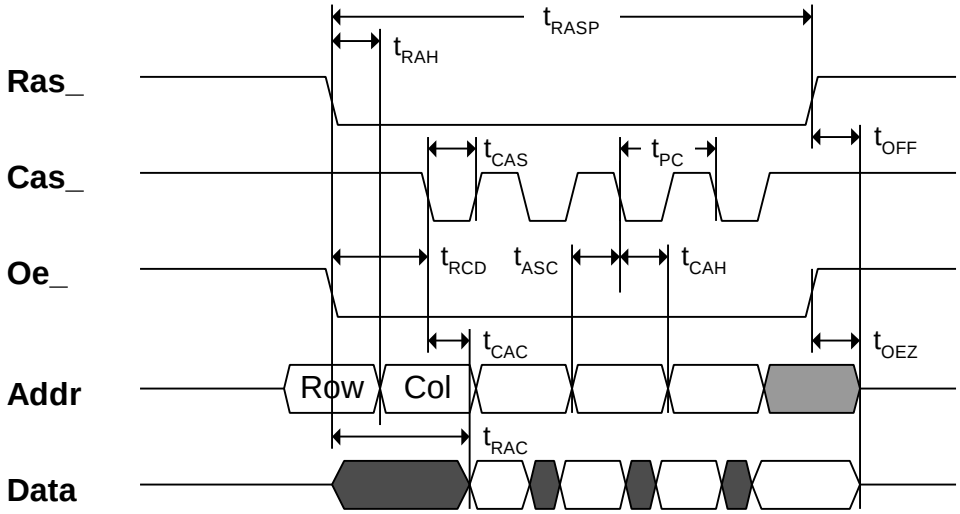


Figure 8. DRAM Interface Refresh Cycle Timing Waveforms

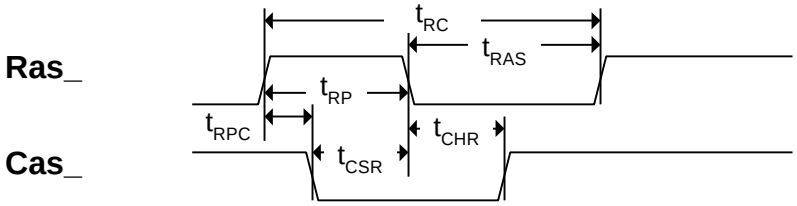


Table 3. Parameters of DRAM Interface Timing

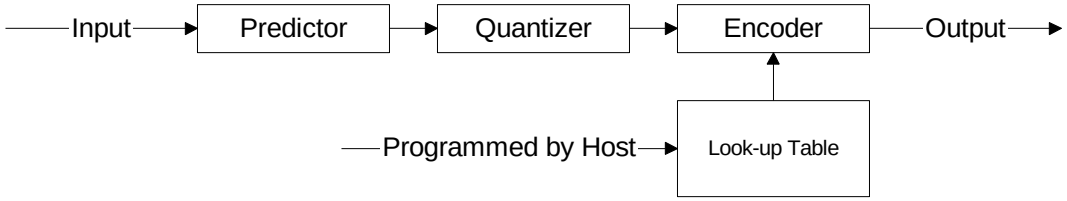
Symbol	Parameter	Min	Max	Unit
t_{RASP}	RAS_ pulse width	185	—	ns
t_{RAH}	Row address hold time	18.5	—	ns
t_{CAS}	CAS_ pulse width	18.5	—	ns
t_{RCD}	RAS_ to CAS_ delay time	39	44	ns
t_{ASC}	Column address setup time	18.5	—	ns
t_{CAH}	Column address hold time	11.5	—	ns
t_{DS}	Data-in setup time	18.5	—	ns
t_{DH}	Data-in hold time	11.5	—	ns
t_{RAC}	Access time from RAS_	—	60	ns
t_{CAC}	Access time from CAS_	—	15	ns
t_{OEZ}	Output buffer turnoff delay form OE_			ns
t_{RPC}	RAS_ precharge to CAS_ hold time	18.5	—	ns
t_{CHR}	CAS_ hold time	55.5	—	ns
t_{CSR}	CAS_ setup time	55.5	—	ns
t_{RC}	Random read or write cycle time	185	—	ns
t_{RAS}	RAS_ pulse width	111	—	ns
t_{RP}	RAS_ precharge time	74	—	ns

2.2.3 OmniCE

OmniCE is a proprietary compression engine, constructed by the predictor, the quantizer, as well as encoder along with look-up tables. The predictor predicts image pixels horizontally and vertically. The outstanding look-up table is programmed by the software driver according to calculation of probability.

The compression ratio of OmniCE varies from 4 to 7, depending on image complexity. Parameters can be modified dynamically by the software driver to achieve the desired frame rate. It can also be disabled and bypass uncompressed data.

Figure 9. Structure of OmniCE



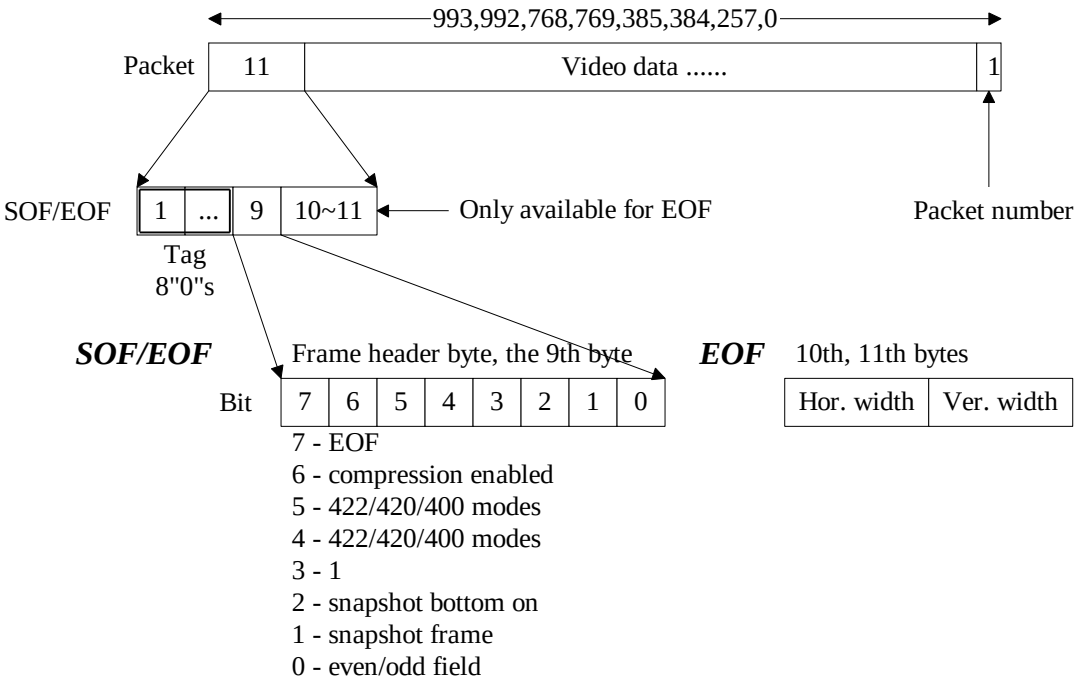
2.2.4 ISO FIFO

OV511 implements one isochronous endpoint for video data transfer. The available alternates include packet size of 0, 257, 512, 513, 768, 769, 992 & 993. The corresponding ISO FIFO size has to be set by the software driver right before the current alternate is set. The size of ISO FIFO is configurable from 32 to 992 in increment of 32.

Moreover, in order to assist packet reordering in the host, a packet number inserted at the end of each packet can be turned on. An image frame starts with the SOF packet (Start Of an image Frame), as well as ends with the EOF packet (End Of an image Frame). The packet number counts up from 01 to 255 and back to 01. Only the SOF packet uses the packet number 00.

SOF/EOF packets are indicated by the unique combination which the 1st to the 8th byte are all "0"s and the 9th byte contains a non-zero header. This header contains image information, such as the operating mode, snapshot flag & even/odd field. In the case of the EOF packet, the 10th and 11th bytes also contain the image width and height information.

Figure 10. SOF/EOF Formats



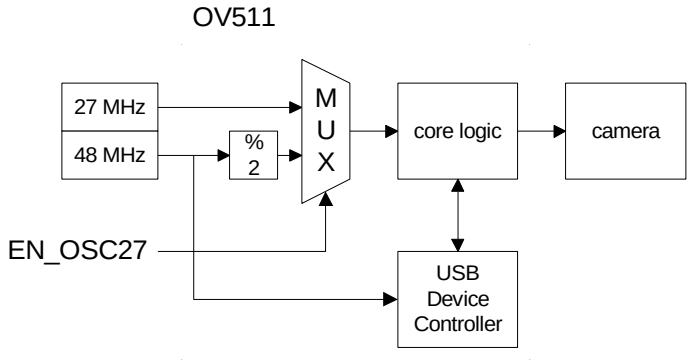
2.2.5 UDC interface

UDC interface performs hand-shaking protocols with USB Device Controller. Its function includes isochronous transfer, responding vendor commands & descriptors, and generating read/write cycles to internal registers.

2.2.6 System Control

System control unit performs functions of system clock generation, Power On Reset, software reset scheme, USB Reset command, system initialization, snapshot and USB suspend.
OV511 takes dual clock inputs, “CLK_48M” & “CLK_27M”. “CLK_48M” takes 48MHz oscillator/crystal input for USB bus, while “CLK_27M” is camera dependent & pin option selectable. 27MHz crystal/oscillator is recommended for VGA resolution cameras to perform frame rate of 30fps. If pin “EN_OSC27” is pulled up, “CLK_27M” is chosen in support of camera clock. If it’s pulled down, “CLK_48M” is divided by 2 and provides camera clock.

Figure 11. Clock Scheme of OV511

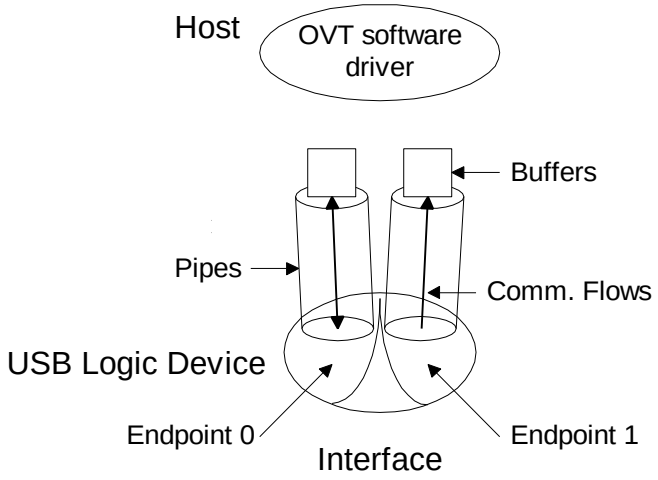


There are three kinds of reset scheme supported by OV511. The Power-On Reset (pin “RESETB”) & USB Reset command initialize OV511 & camera circuits. The Camera Reset (pin “RESET”) toggles as soon as either Power-On Reset or USB Reset is asserted. The software reset allows individual functional blocks to be reset without altering the register contents. Software reset is necessary when changing camera formats, ISO packet size, compression parameters, etc.
According to USB specification, a high-power (> 100mA) function requires staged switching of power. It must first come up in a reduced power state of less than one unit load, which is 100mA. System initialization function stops system clocks as well as sets camera into power down mode by using pin “PWDN” before bus enumeration. If sufficient power exists in the power budget, the remainder of the function will be powered on by setting register bit “EN_SYS” (register 53h). In this case, pin “EN_SYSTEM” has to be pulled down. If it’s pulled up, the camera system will be high power function right after Power-On Reset occurs.
The snapshot function can be achieved by either setting register bit “SNAP[2]” (register 52h) or pushing a bottom (pin “SNAPB”) on the system. Hardware snapshot function is initiated by setting register bit “SNAP[0]” (register 52h). Once pushing the bottom, the internal snapshot signal is latched, registers of the camera interface & camera itself are modified to desired formats as well. As soon as OV511 captures one single frame of image and sends to the host, the software driver clears the internal snapshot signal for next snapshot operation by writing a sequence 0-1-0 to register bit “SNAP[1]” (register 52h).
When USB bus idles for more than 3 msec, OV511 goes into suspend mode and all clocks are stopped by pin “OSC_EN”, while all internal registers are remained the same values. The system wakes up when the USB resume condition occurs. Suspend function can be disabled by pulling down pin “EN_SUSPEND”, while pin “OSC_EN” can be disabled by pulling up pin “OSC_BYPASS”.

2.2.7 USB Device Controller

The camera system constructed by OV511 is defined as a “high-power, bus-powered” USB device. It means that the camera system draws over one and a maximum of five unit loads from the USB cable. Two endpoints are implemented for communication flows between the USB camera device and the USB host. Endpoint 0 is an In-Out type CONTROL endpoint which is the pipe of Descriptors, Configurations and Vendor Commands (internal registers). Endpoint 1 is an In type Isochronous endpoint which is the pipe of video streams.

Figure 12. USB Communication Flow



The USB Descriptors are configured as one configuration, one interface and eight alternates. The packet sizes of eight alternates are 992, 993, 768, 769, 512, 513, 257 & 0.
There is no built-in USB transceiver in OV511. Therefore, the USB transceiver is required on the camera system. The camera system is defined as a full speed device and needs to be terminated with the pull-up resistor on the D+ line.

2.2.8 I^2C

A built-in I^2C bus master with two dedicated pins “SCL” & “SDA” controls cameras. Pin “SDA” is an open drain I/O, while pin “SCL” is an output only. Each pin requires a 4.7K pull-up resistor to 5V. The data rate of the I^2C bus master is programmable and the maximum data rate is 100K.

Figure 13. A Complete Data Transfer on I^2C Bus

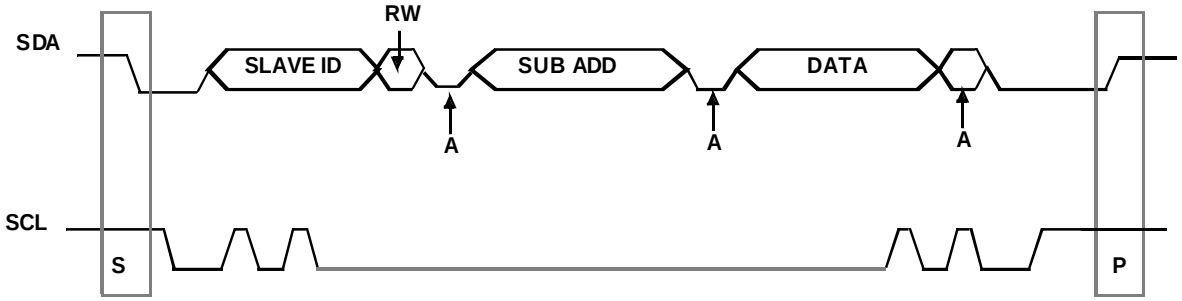
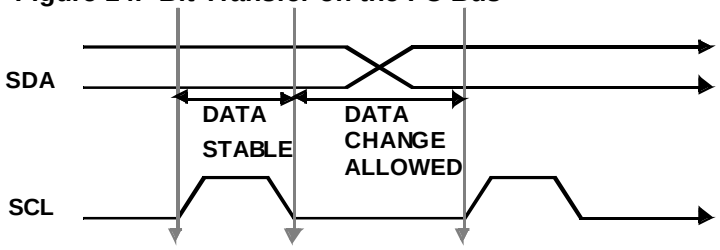


Figure 14. Bit Transfer on the I²C Bus



2.2.9 PIO

PIO is a parallel I/O port for accessing external SRAM based devices. It has a standard memory like interface that requires address, data and read/write control signals. These signals share the same buses with the Y and UV video channels. When PIO is enabled, Y channel becomes the PIO data bus for both input and output modes, and UV channel becomes address bus and read/write control signals. In this case, video data inputs will be interrupted. The pin assignment of PIO control signals is as following,

- UV [5:0] share with ADDR [5:0], any arbitrary address can be defined by users as CSB
- UV [6] shares with WEB
- UV [7] shares with OEB

Figure 15. PIO Read Cycle Timing Waveforms

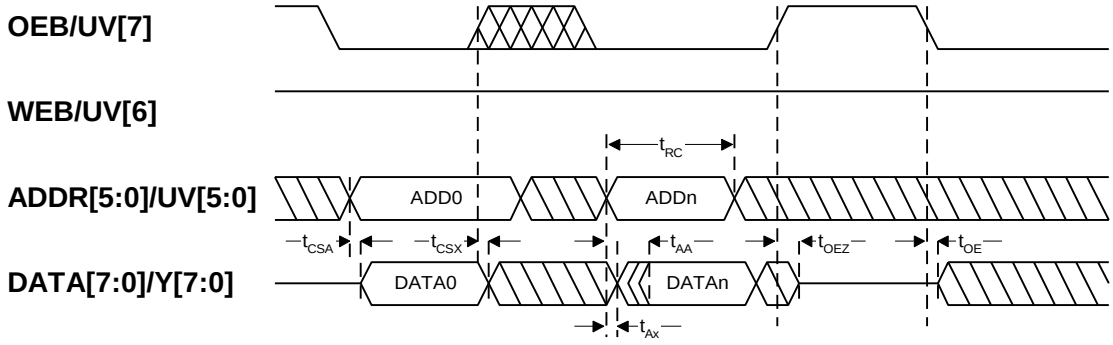


Figure 16. PIO Write Cycle Timing Waveforms

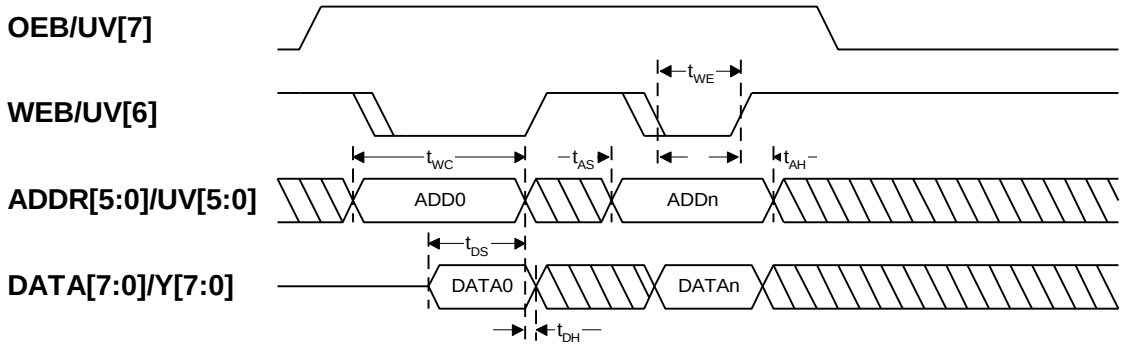


Table 4. Parameters of PIO Timing

Symbol	Parameter	Min	Max	Unit
T_{OE}	Output enable access time	15	—	ns

Parameters of PIO Timing (continued)

T_{OEZ}	Output enable to z delay	15	—	ns
T_{RC}	Register read cycle time	—	100	ns
T_{CSA}	Chip select access time	30	—	ns
T_{CSX}	Chip select to data invalid time	15	—	ns
T_{AA}	Address access time	30	—	ns
T_{AX}	Address data invalid time	15	—	ns
T_{WC}	Register write cycle time	—	100	ns
T_{WE}	Write enable pulse width	—	50	ns
T_{AS}	Write cycle address set up time	—	0	ns
T_{AH}	Write cycle address hold time	—	0	ns
T_{DS}	Write cycle data set up time	—	20	ns
T_{DH}	Write cycle data hold time	—	0	ns

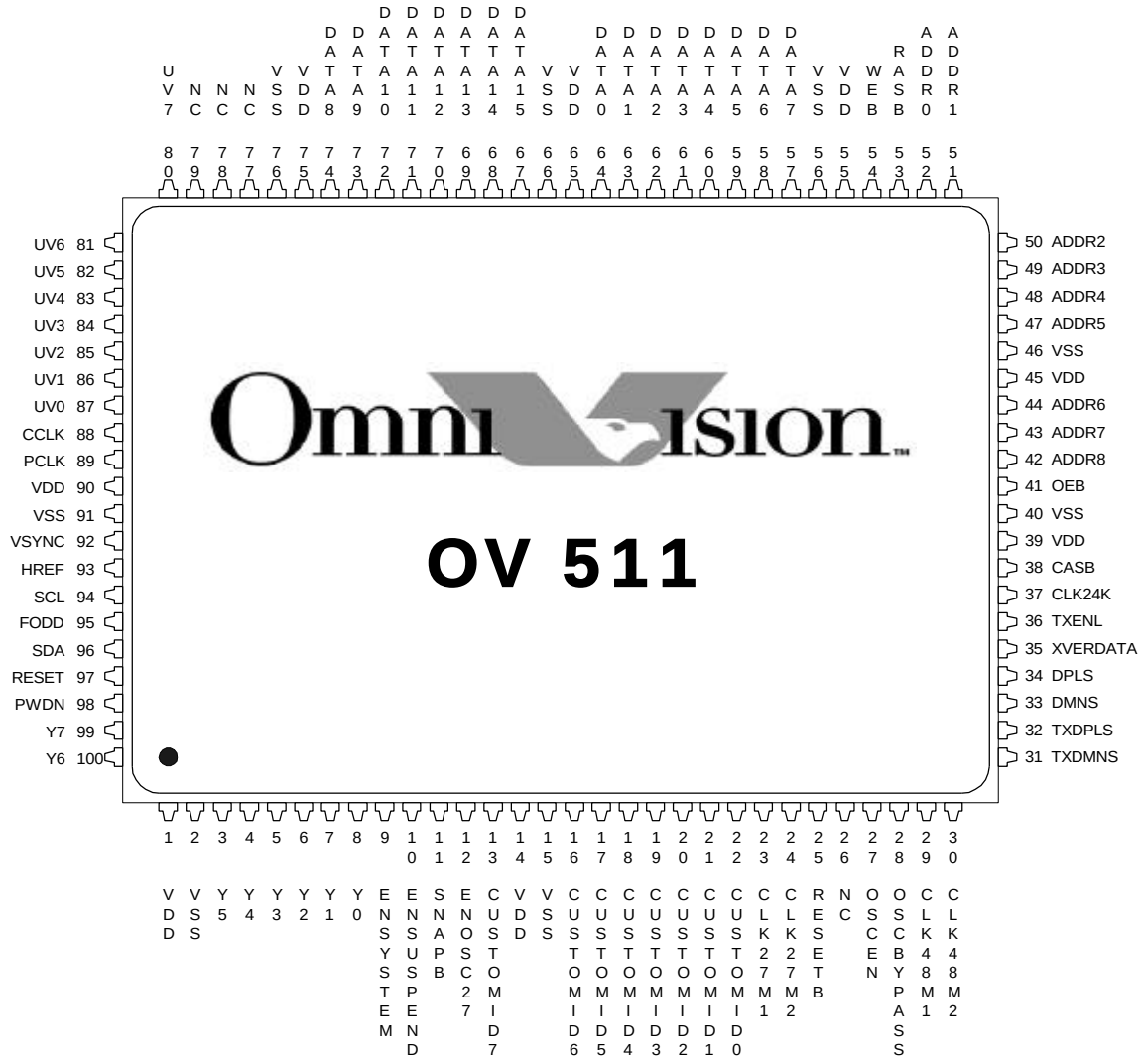
2.2.10 Custom ID

Custom ID is a specific 8-bit input port which can be pulled up/down to identify company names of manufacturers. The Custom ID is checked by the software driver and may be requested directly from OVT. If no Custom ID is applied, pull-up/down resistors are also required to avoid bus floating.

3 Pin Definition

3.1 Pin Assignments

Figure 17. 100-Pin PQFP Package



3.2 Pin Descriptions

Table 5. Pin Descriptions

Items/Pin #	Name	I/O	Function
Camera Interface			
99, 100, 3~8	Y[7:0]	I/O	Camera Y data input
			PIO data input/output
80~87	UV[7:0]	I/O	Camera UV data input
			PIO address, read/write control output
89	PCLK	I	Camera pixel clock input
93	HREF	I	Camera horizontal window reference input
92	VSYNC	I	Camera vertical sync. input
95	FODD	I	Camera even/odd field flag input
88	CCLK	O	Camera clock output. Software programmable
97	RESET	O	Camera hardware reset output
98	PWDN	O	Camera power down output
I^2C Interface			
96	SDA	I/O	I^2C serial data. Pull-up resistor (4.7K Ohm) is required
			Bi-directional with open-drain output
94	SCL	O	I^2C serial clock output. Pull-up resistor (4.7K Ohm) is required
DRAM Interface			
67~74, 57~64	DATA[15:0]	I/O	DRAM 16-bit data
41	OEB	O	DRAM OE_ output
54	WEB	O	DRAM WE_ output
42~44, 47~52	ADDR[8:0]	O	DRAM address output
38	CASB	O	DRAM CAS_ output
53	RASB	O	DRAM RAS_ output
USB Interface			
35	XVER_DATA	I	USB differential receiver data input
33	DMNS	I	D- input
34	DPLS	I	D+ input
36	TXENL	O	Output enable for differential driver
31	TXDMNS	O	NRZI formatted D- output
32	TXDPLS	O	NRZI formatted D+ output
Clock & Misc.			
25	RESETB	I	Power-On Reset input. Low-active
29	CLK_48M1	I	48MHz oscillator/crystal input
30	CLK_48M2	O	48MHz crystal output
23	CLK_27M1	I	27MHz oscillator/crystal input
24	CLK_27M2	O	27MHz crystal output
27	OSC_EN	O	Power control for oscillator. 1 for power enabled
28	OSC_BYPASS	I	OSC_EN enabled/disabled input. 0 for enabled
11	SNAPB	I	Snapshot bottom input. Cleared by the software driver
9	EN_SYSTEM	I	Hardware system initialization enabled/disabled. 0 for disabled
10	EN_SUSPEND	I	Hardware suspend enabled/disabled. 1 for enabled
13, 16~22	CUSTOM_ID[7:0]	I	Custom ID inputs
12	EN_OSC27	I	27MHz clock input select. 1 for enabled
37	CLK_24K	O	24KHz clock output for switching power supply

Pin Descriptions (continued)

Items/Pin #	Name	I/O	Function
Power & Ground			
1, 14, 39, 45, 55, 65	VDD	I	Power
75, 90			
2, 15, 40, 46, 56, 66	VSS	I	Ground
76, 91			
Others			
26, 77, 78, 79	NC		

4 Electrical Characteristics

Table 6. DC Electrical Characteristics
V_{DD} = 5V ± 5%, TA = 0 to 70°C

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	High level input voltage		2.0 (TTL) ~ 4.0 (CMOS schmitt trigger)		V
V_{IL}	Low level input voltage			0.8~1.0	V
I_{IH}	High level input current	$V_{IN} = V_{DD}$	-10	10	uA
I_{IL}	Low level input current	$V_{IN} = V_{SS}$	-10	10	uA
V_{OH}	High level output voltage		2.4		V
V_{OL}	Low level output voltage			0.4	V
I_{OZ}	Tri-state output leakage current	$V_{OUT} = V_{SS}$ or V_{DD}	-10	10	uA
I_{DD}	Quiescent supply current	$V_{IN} = V_{SS}$ or V_{DD}		100	uA

Table 7. Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	-0.3 to 7	V
V_{IN}	DC input voltage	-0.3 to V_{DD} + 0.3	V
I_{IN}	DC input current	± 10	mA
T_{STG}	Storage temperature	-40 to 125	°C

Table 8. Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage 5V	4.75 to 5.25	V
T_A	Commercial temperature	0 to 70	°C

5 Register Table (Vendor Commands)

5.1 CAMERA INTERFACE

Table 9. Camera Interface Register List

Register Address	Register Name	R/W	Function	Default Value
10h	DLYM[1:0]	RW	Bit 1~0 : Delay modes of video input signals 00 : no delay 01 : delays YUV by one PCLK 10 : delays HREF by one PCLK 11 : delays YUV and HREF by one PCLK	00h
11h	PEM[0]	RW	Bit 0 : Edge modes of PCLK 0 : PCLK negative edge latches video data 1 : PCLK positive edge latches video data	01h
12h	PXCNT[6:0]	RW	Bit 6~0 : Clamped pixel number It defines the clamped pixel number of a horizontal line in increment of 8 pixels. If the pixel number from camera is larger than this number, the spare pixels will be dropped. Clamped Pixel No. = (PXCNT + 1) * 8	27h
13h	LNCNT[6:0]	RW	Bit 6~0 : Clamped line number It defines the clamped line number in increment of 8 lines. If the line number from camera is larger than this number, the spare lines will be dropped. Clamped Line No. = (LNCNT + 1) * 8	1Dh
14h	PXDV[1:0]	RW	Bit 1~0 : Pixel divisor It defines down sampling frequency in the horizontal pixel direction. 00 : divided by 1 01 : divided by 2 10 : divided by 4 11 : divided by 8	01h
15h	LNDV[1:0]	RW	Bit 1~0 : Line divisor It defines down sampling frequency in the vertical line direction. Uses these register bits along with register bit LSTR to retain even or odd lines. 00 : divided by 1 01 : divided by 2 10 : divided by 4 11 : divided by 8	01h
16h	M400[0]	RW	Bit 0 : 8 bit (Y channel only) / 16 bit (Y & UV channels) data input select 0 : 8 bit data in Y channel (UV channel is ignored) 1 : 16 bit data in both Y & UV channels. Uses this register bit along with register bit M420 to select 422/420 formats.	01h
17h	LSTR[0]	RW	Bit 0 : Reserved lines for downing sampling 0 : even lines (2, 4, 6, 8, ……) 1 : odd lines (1, 3, 5, 7, ……)	00h
18h	M420[1] YFIR[0]	RW	Bit 1 : YUV422/420 0 : YUV 4:2:2 1 : YUV 4:2:0 Bit 0 : Y channel low pass filter 0 : disabled 1 : enabled	00h

- **Snapshot Operation –** a full set of camera interface registers are duplicated for hardware snapshot operation. These registers replace the normal ones for taking snapshot frame so that the snapshot frame can be different settings from normal frame. The followings are the snapshot registers.

Camera Interface Register List (continued)

Register Address	Register Name	R/W	Function	Default Value
19h	SPDLY[7:0]	RW	Bit 7~0 : Captured frame for snapshot It defines which frame (one frame only) after snapshot function is triggered will be captured. 00000000 : the first frame 10000001 ~ 11111111 : the 2^{nd} ~ 128^{th} frame	00h
1Ah	SNPX[6:0]	RW	Bit 6~0 : Clamped pixel number for snapshot	4Fh
1Bh	SNLN[6:0]	RW	Bit 6~0 : Clamped line number for snapshot	1Dh
1Ch	SNPD[1:0]	RW	Bit 1~0 : Pixel divisor for snapshot	00h
1Dh	SNLD[1:0]	RW	Bit 1~0 : Line divisor for snapshot	01h
1Eh	SN400[0]	RW	Bit 0 : 8/16 bit data input for snapshot	01h
1Fh	SNALSTR[2] SN420[1] SNYFIR[0]	RW	Bit 2 : Reserved lines for down sampling when snapshot occurs Bit 1 : YUV422/420 for snapshot Bit 0 : Y channel low pass filter for snapshot	04h

5.2 DRAM INTERFACE

Table 10. DRAM Interface Register List

Register Address	Register Name	R/W	Function	Default Value
20h	ENFC[0]	RW	Bit 0 : Image flow control 0 : disabled, doesn't guarantee a complete image frame 1 : enabled, guarantees a complete image frame	01h
21h	ARCP[0]	RW	Bit 0 : Auto read cycle predictor It predicts the number of read cycles which will be inserted besides write cycles. 0 : disabled, use register bit MRC for manual setting 1 : enabled	01h
22h	MRC[3:0]	RW	Bit 3~0 : Manual read cycle insertion It defines the number of read cycles which will be inserted besides write cycles. Read cycles = MRC + 1	01h
23h	RFC[5:0]	RW	Bit 5~0 : Refresh counter	1Ah

5.3 ISO FIFO

Table 11. ISO FIFO Register List

Register Address	Register Name	R/W	Function	Default Value
30h	PKSZ[4:0]	RW	Bit 4~0 : Packet size It defines the packet size of ISO FIFO which is available from 00001 (32 bytes) to 11111 (992 bytes). The packet size must match with the current alternate setting. Packet size = (32 * PKSZ) bytes	08h
31h	NZPK[3] ENPKNO[1] ENCE[0]	RW	Bit 3 : Zero packet inserted after EOF (image end of frame flag) 0 : disabled 1 : enabled Bit 1 : Packet No. insertion It inserts one extra byte at the end of each packet as the packet number. It counts in sequence, but only the packet containing SOF (image start of frame flag) uses "00". 0 : disabled 1 : enabled Bit 0 : Compressed data non-zero (01) insertion It inserts "01" at the 7^{th} byte of the packet if the 1^{st} ~8^{th} incoming compressed data are all "00". 0 : enabled 1 : disabled	03h

5.4 PIO

Table 12. PIO Register List

Register Address	Register Name	R/W	Function	Default Value
38h	ENPIO[7] PIORW[6] PADD[5:0]	W	Bit 7 : Parallel IO operation 0 : disabled 1 : enabled. UV channel changes to output mode for parallel IO operation. Register bits PADD[5:0] output to pin UV[5:0]. UV[6] performs as OEB, while UV[7] performs as WEB. Y channel is bi-directional. The direction depends on read/write operation of PIO. The bus cycle is executed once only after USB host write to this register and ENPIO = 1. Write data has to be placed in register bits PDATA[7:0] before launching the PIO write cycle. Read data is returned in register bits PDATA[7:0] after launching the PIO read cycle. Bit 6 : Read/write cycle for PIO operation 0 : read cycle 1 : write cycle Bit 5~0 : address port of PIO operation	00h
39h	PDATA[7:0]	R/W	Bit 7~0 : data port of PIO operation	00h
3Eh	ENTP[3] TPS[2:0]	W	Bit 3 : BIST operation for OV511 0 : disabled 1 : enabled Bit 2~0 : BIST functions select	00h

- **PIO R/W sequence examples**

Write cycles

1. Writes to data port (PDATA, register 39h)
2. Enables PIO (ENPIO, register 38h), sets up address (PADD, register 38h), & selects write cycle (PIORW, register 38h)
3. Disables PIO (ENPIO, register 38h)

Read cycles

1. Enables PIO (ENPIO, register 38h), sets up address (PADD, register 38h), & selects read cycle (PIORW, register 38h)
2. Reads from data port (PDATA, register 39h)

5.5 I^2C

Table 13. I^2C Register List

Register Address	Register Name	R/W	Function	Default Value
40h	TMOUT[2] NOACK[1] IDLE[0]	R	Bit 2 : Time out flag for I^2C operation. Sets when timer reaches the value set by register bits TMO[4:0]. Bit 1 : No acknowledge on I^2C bus. It's valid when register bit IDLE is set. Bit 0 : I^2C bus idle flag	00h
40h	ENABORT[4] TYPE[2:1] STARTI2C[0]	W	Bit 4 : Aborts I^2C bus cycle if I^2C slave doesn't response (no acknowledge) Bit 2~1 : Types of I^2C read/write sequence 00 : 3 byte write cycle, in sequence of slave ID (SID), sub address (SWA) & I^2C data (SDA) 01 : 2 byte write cycle, in sequence of slave ID (SID) & sub address (SMA) 1x : 2 byte read cycle, in sequence of slave ID (SRA) & I^2C data (SDA) Bit 0 : Launches a new I^2C bus cycle if set I^2C won't launch a new cycle if it doesn't finish the previous bus cycle.	00h
41h	SID[7:0]	RW	Bit 7~0 : I^2C slave ID for 3 or 2 byte write cycles	00h

I²C Register List (continued)

Register Address	Register Name	R/W	Function	Default Value
42h	SWA[7:0]	RW	Bit 7~0 : Sub address for 3 byte write cycles	00h
43h	SMA[7:0]	RW	Bit 7~0 : Sub address for 2 byte write cycles	00h
44h	SRA[7:0]	RW	Bit 7~0 : Slave ID for 2 byte read cycles	00h
45h	SDA[7:0]	RW	Bit 7~0 : I²C read/write data port	00h
46h	PSC[7:0]	RW	Bit 7~0 : I²C clock prescaler It defines prescaler values for I²C clock. I²C bit rate = 93.5 KHz / (PSC + 1)	00h
47h	TMO[4:0]	RW	Bit 4~0 : Time out counter A timer starts to count I²C clocks when I²C bus cycle is launched. When the timer reaches TMO, TMOUT is set.	00h

- **Snapshot Operation -** During the period of hardware snapshot operation, OV511 first launches a 3 byte I²C write cycle to I²C slave device, such as camera, by using register 48h and 49h. It permits I²C slave device to modify the internal settings before taking the snapshot.

I²C Register List (continued)

Register Address	Register Name	R/W	Function	Default Value
48h	SPA[7:0]	W	Bit 7~0 : Sub address of the I²C write cycle for snapshot operation	00h
49h	SPD[7:0]	W	Bit 7~0 : Data port of the I²C write cycle for snapshot operation	00h

- **I²C R / W Sequence Examples**

Setup stage

1. Writes to slave ID (SID, register 41h)

3 byte write cycles

1. Writes to sub address (SWA, register 42h)
2. Writes to data port (SDA, register 45h)
3. Writes to control bits to select write cycle and launch I²C cycles (TYPE, STARTI2C, register 40h)

2 byte dummy write cycles (In order to set sub address of I²C slave device for the next coming read cycle)

1. Writes to sub address (SMA, register 43h)
2. Writes to control bits to select write cycle and launch I²C cycles (TYPE, STARTI2C, register 40h)

2 byte read cycles

1. Writes to sub address (SRA, register 44h)
2. Writes to control bits to select read cycle and launch I²C cycles (TYPE, STARTI2C, register 40h)
3. Reads from status bits (TMOUT, NOACK, IDLE, register 40h)
4. Reads from data port (SDA, register 45h)

5.6 SYSTEM CONTROL

Table 14. System Control Register List

Register Address	Register Name	R/W	Function	Default Value
50h	RST[6:0]	RW	Bit 0 : Software reset for UDC Bit 1 : Software reset for I^2C Bit 2 : Software reset for ISO FIFO Bit 3 : Software reset for OmniCE Bit 4 : Software reset for DRAM interface Bit 5 : Software reset for camera interface Bit 6 : Software reset for OV511 & registers	00h
51h	CLKDIV[4:0]	RW	Bit 4~0 : Camera clock divisor It defines the frequency of camera clock output CCLK. CCLK is divided down based on external clock inputs CLK_48 or CLK_27. The maximum frequency of CLK_27 that OV511 can handle is 27MHz. If both CLK_27 and CLK_48 clock inputs are enabled by pulling up pin “EN_OSC27”, CLK_27 is chosen in support of camera clock. 00000 : no division (CLK_27) 11111 : CLK_27 divided by 32 If only CLK_48 clock input is enabled by pulling down pin “EN_OSC27”, CLK_48 is divided by 2 and provides camera clock.	00h
52h	SNAP[2:0]	RW	Bit 0 : Hardware snapshot 0 : disabled 1 : enabled Bit 1 : Releases hardware snapshot bottom in sequence of 0,1,0 Bit 2 : Software snapshot 0 : disabled 1 : enabled	01h
53h	EN_SYS[0]	RW	Bit 0 : Software system initialization Before system is initialized, system clocks will be stopped to meet the requirement of power consumption for the whole system to be less than 100mA. After that, it can increase to max. 500mA for USB bus powered device. If pin “EN_SYSTEM” is pulled down, this bit controls system initialization. Otherwise, system is initialized right after power-on reset. 0 : system is not initialized 1 : system is initialized	00h
5Eh	USR[7:0]	RW	Bit 7~0 : User defined read/write register bits	00h
5Fh	CID[7:0]	R	Bit 7~0 : Custom ID which links to input pins “CUSTOM_ID” It is checked by the software driver to identify company names. It may be requested directly from OVT. The registered custom ID can be coded by pulling up or down resistors through pins “CUSTOM ID”. If no custom ID is applied, pull-up/down resistors are also requested to avoid floating.	~

5.7 OmniCE

Table 15. OmniCE Register List

Register Address	Register Name	R/W	Function	Default Value
70h	PRH_Y[5:0]	RW	Bit 5~0 : Predication range in horizontal direction for Y channel One horizontal line is divided into horizontal segments for prediction. It defines the number of pixels contained in one horizontal segment of Y channel. Pixels in the segment except the first one are predicted by the first pixel of this segment.	1Fh
71h	PRH_UV[5:0]	RW	Bit 5~0 : Prediction range in horizontal direction for UV channel	05h

OmniCE Register List (continued)

72h	PRV_Y[7:0]	RW	Bit 7~0 : Predication range in vertical direction for Y channel One image frame is divided into vertical segments for prediction. It defines the number of pixels contained in one vertical segment of Y channel. Pixels in the segment except the first one are predicted by the first pixel of this segment.	06h
73h	PRV_UV[7:0]	RW	Bit 7~0 : Predication range in vertical direction for UV channel	06h
74h	QTH_Y[7:0]	RW	Bit 7~0 : Quantization threshold in horizontal direction for Y channel	14h
75h	QTH_UV[7:0]	RW	Bit 7~0 : Quantization threshold in horizontal direction for UV channel	03h
76h	QTV_Y[7:0]	RW	Bit 7~0 : Quantization threshold in vertical direction for Y channel	04h
77h	QTV_UV[7:0]	RW	Bit 7~0 : Quantization threshold in vertical direction for UV channel	04h
78h	UV_en[2] Y_en[1] CE_en[0]	RW	Bit 0 : OmniCE 0 : disabled 1: enabled Bit 1 : Y channel operation 0 : disabled 1 : enabled Bit 2 : UV channel operation 0 : disabled 1 : enabled	06h
79h	LTEN_UV[1] LTEN_Y[0]	RW	Bit 0 :Look-up table for Y channel 0 : disabled 1 : enabled Bit 1 : Look-up table for UV channel 0 : disabled 1 : enabled	00h
80~9Fh	LT_Y	RW	Bit 7~0 : Programmable look-up table for Y channel	~
A0~BFh	LT_UV	RW	Bit 7~0 : Programmable look-up table for UV channel	~

6 USB Descriptors

The USB descriptor is a data structure with defined attributes that can respond requests from the USB host. The descriptors of OV511 are hardwire coded inside the chip, and no external EPROM is required.

6.1 Device

The device descriptor describes general information about OV511. There is one device descriptor.

Table 16. Device Descriptor List

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	12	Size of descriptor in bytes
1	BdescriptorType	1	01	DEVICE Descriptor Type
2	BcdUSB	2	0100	USB Spec Release No.
4	BdeviceClass	1	00	Class code
5	BdeviceSubClass	1	00	Subclass code
6	BdeviceProtocol	1	00	Protocol code
7	BmaxPacketSize0	1	08	Max. packet size for enpt0
8	IdVendor	2	05a9	Vendor ID
10	IdProduct	2	0511	Product ID
12	BcdDevice	2	0100	Device release No.
14	Imanufacturer	1	00	Index of string descriptor describing manufacturer
15	Iproduct	1	00	Index of string descriptor describing product
16	IserialNumber	1	00	Index of string descriptor describing the device's serial no.
17	BnumConfigurations	1	01	Number of possible configurations

6.2 Configuration

The configuration descriptor describes information about a specific device configuration. There is one configuration descriptor.

Table 17. Configuration Descriptor List

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	02	CONFIGURATION
2	WtotalLength	2	0089	Total length of data returned for this configuration
4	BnumInterfaces	1	01	No. of interfaces supported by this config.
5	BconfigurationValue	1	01	Value to use to Set Config. to select this config.
6	Iconfiguration	1	00	Index of string descriptor describing this config.
7	BmAttributes	1	80	Config. char. bus powered, no remote wakeup
8	MaxPower	1	FA	Max. power consumption, 500 ma

6.3 Interface & Endpoint

The interface descriptor describes a specific interface provided by the associated configuration. There are eight interface descriptors. Each one selects one alternate setting and is followed by the corresponding endpoint descriptor.

The endpoint descriptor describes the information required by the host to determine the bandwidth requirements of each endpoint. There is no endpoint descriptor for endpoint zero.

6.3.1 Alternate 0

Table 18. Interface Descriptor List of Alternate 0

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE
2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	00	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code
6	BinterfaceSubClass	1	00	SubClass code
7	BinterfaceProtocol	1	00	Protocol code
8	Iinterface	1	00	Index of string descriptor describing this interface

Table 19. Endpoint Descriptor List of Alternate 0, Packet Size 992

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso
4	WmaxPacketSize	2	03E0	Max. packet size 992
6	Binterval	1	01	Interval for polling enpt for data transfer

6.3.2 Alternate 1

Table 20. Interface Descriptor List of Alternate 1

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE
2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	01	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code
6	BinterfaceSubClass	1	00	SubClass code
7	BinterfaceProtocol	1	00	Protocol code
8	Iinterface	1	00	Index of string descriptor describing this interface

Table 21. Endpoint Descriptor List of Alternate 1, Packet Size 993

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso
4	WmaxPacketSize	2	03E1	Max. packet size 993
6	Binterval	1	01	Interval for polling enpt for data transfer

6.3.3 Alternate 2

Table 22. Interface Descriptor List of Alternate 2

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE
2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	02	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code
6	BinterfaceSubClass	1	00	SubClass code

Interface Descriptor List of Alternate 2 (continued)

7	BinterfaceProtocol	1	00	Protocol code
8	Iinterface	1	00	Index of string descriptor describing this interface

Table 23. Endpoint Descriptor List of Alternate 2, Packet Size 768

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso
4	WmaxPacketSize	2	0300	Max. packet size 768
6	Binterval	1	01	Interval for polling enpt for data transfer

6.3.4 Alternate 3

Table 24. Interface Descriptor List of Alternate 3

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE
2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	03	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code
6	BinterfaceSubClass	1	00	SubClass code
7	BinterfaceProtocol	1	00	Protocol code
8	Iinterface	1	00	Index of string descriptor describing this interface

Table 25. Endpoint Descriptor List of Alternate 3, Packet Size 769

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso
4	WmaxPacketSize	2	0301	Max. packet size 769
6	Binterval	1	01	Interval for polling enpt for data transfer

6.3.5 Alternate 4

Table 26. Interface Descriptor List of Alternate 4

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE
2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	04	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code
6	BinterfaceSubClass	1	00	SubClass code
7	BinterfaceProtocol	1	00	Protocol code
8	Iinterface	1	00	Index of string descriptor describing this interface

Table 27. Endpoint Descriptor List of Alternate 4, Packet Size 512

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso
4	WmaxPacketSize	2	0200	Max. packet size 512

Endpoint Descriptor List of Alternate 4, Packet Size 512 (continued)

6	Binterval	1	01	Interval for polling enpt for data transfer

6.3.6 Alternate 5

Table 28. Interface Descriptor List of Alternate 5

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE
2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	05	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code
6	BinterfaceSubClass	1	00	SubClass code
7	BinterfaceProtocol	1	00	Protocol code
8	Iinterface	1	00	Index of string descriptor describing this interface

Table 29. Endpoint Descriptor List of Alternate 5, Packet Size 513

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso
4	WmaxPacketSize	2	0201	Max. packet size 513
6	Binterval	1	01	Interval for polling enpt for data transfer

6.3.7 Alternate 6

Table 30. Interface Descriptor List of Alternate 6

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE
2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	06	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code
6	BinterfaceSubClass	1	00	SubClass code
7	BinterfaceProtocol	1	00	Protocol code
8	Iinterface	1	00	Index of string descriptor describing this interface

Table 31. Endpoint Descriptor List of Alternate 6, Packet Size 257

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso
4	WmaxPacketSize	2	0101	Max. packet size 257
6	Binterval	1	01	Interval for polling enpt for data transfer

6.3.8 Alternate 7

Table 32. Interface Descriptor List of Alternate 7

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE

Interface Descriptor List of Alternate 7 (continued)

2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	07	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code
6	BinterfaceSubClass	1	00	SubClass code
7	BinterfaceProtocol	1	00	Protocol code
8	Iinterface	1	00	Index of string descriptor describing this interface

Table 33. Endpoint Descriptor List of Alternate 7, Packet Size 0

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso
4	WmaxPacketSize	2	0000	Max. packet size 0
6	Binterval	1	01	Interval for polling enpt for data transfer

7 Software Package

The followings are software drivers that are or will be supported by OVT.

- **Stream Class MiniDriver -** A WDM (Microsoft Win32 Driver Model) stream class driver that supports the OVT USB camera system in the Microsoft Windows 98 and Windows NT 5.0. This driver is the bottom level of the software system, and it completes all actual control actions.

- **Video for Windows Compatible Driver** - The VFW is the standard interface of Microsoft for Video Capture drivers. Package contains a VFW-to-WDM mapper extension DLL. It adds some pages in Video source property control dialog. This driver allows user control every custom property.

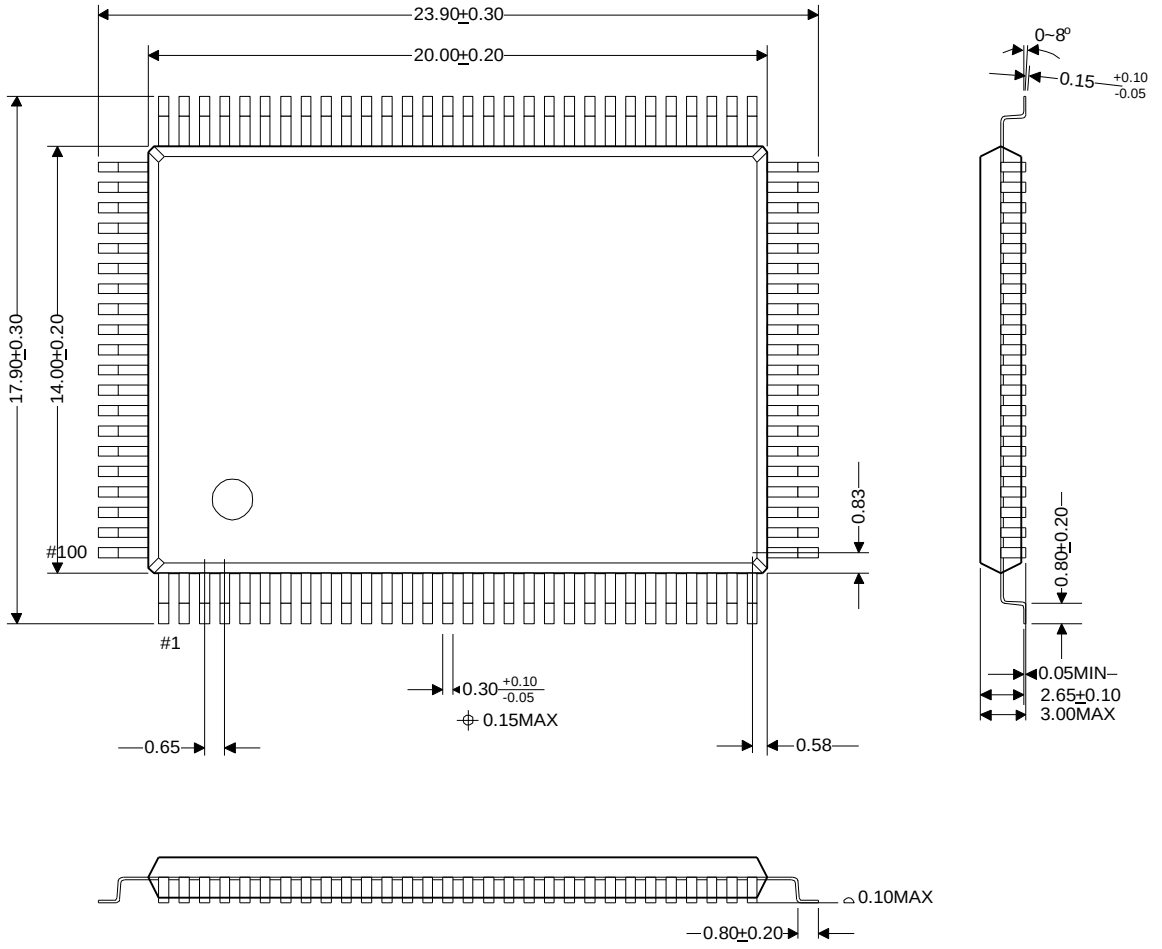
- **TWAIN Source Control Driver** - This driver is compatible with Microsoft still image architecture in Windows 98. It allows standard still image oriented application which use the TWAIN API to use the OVT USB Camera system.

- **DirectShow Filter** - This software component allows users to control every custom property in DirectShow graph.

- **Installation Software** - The installation software is responsible for setting up all camera software components.

8 Mechanical Information

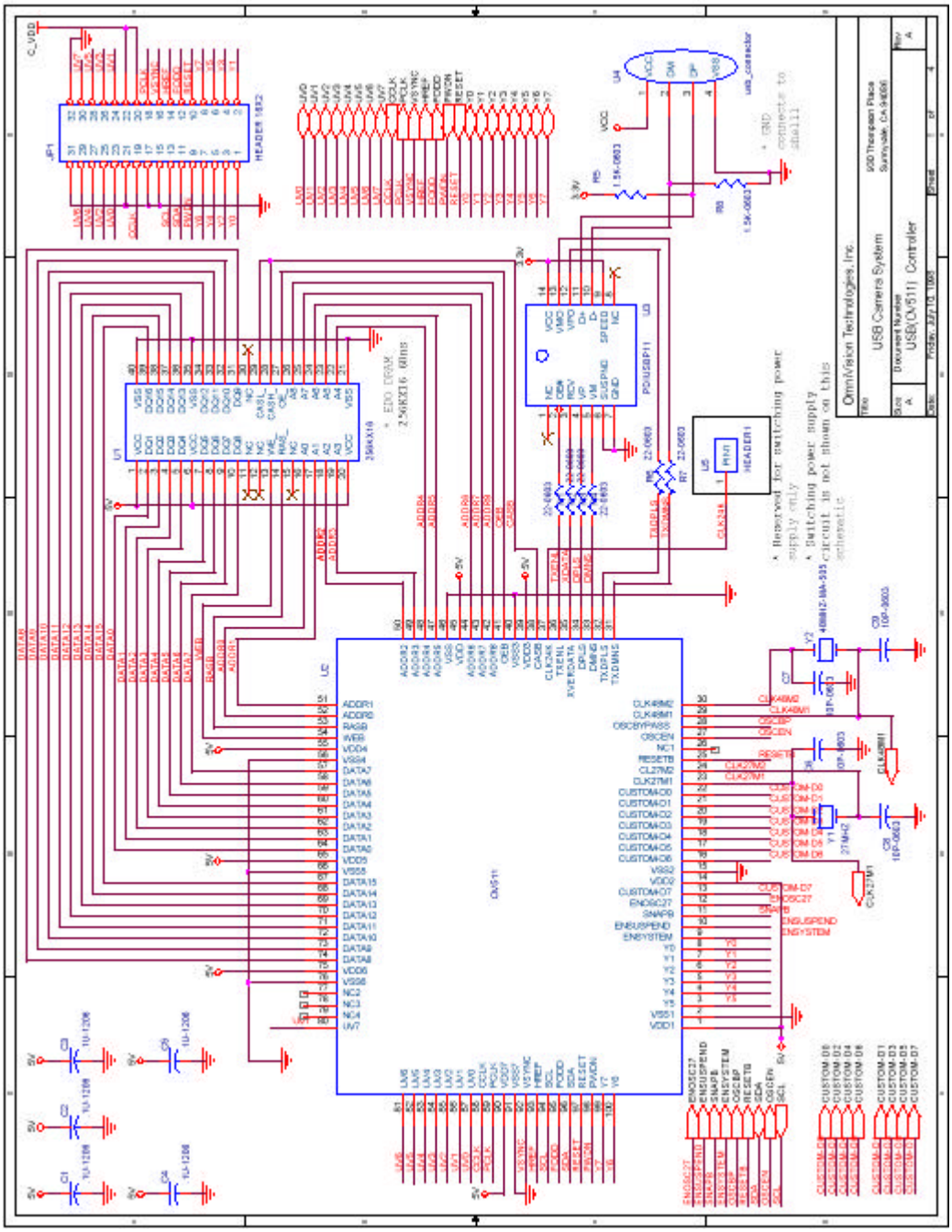
Dimensions in Milimeters



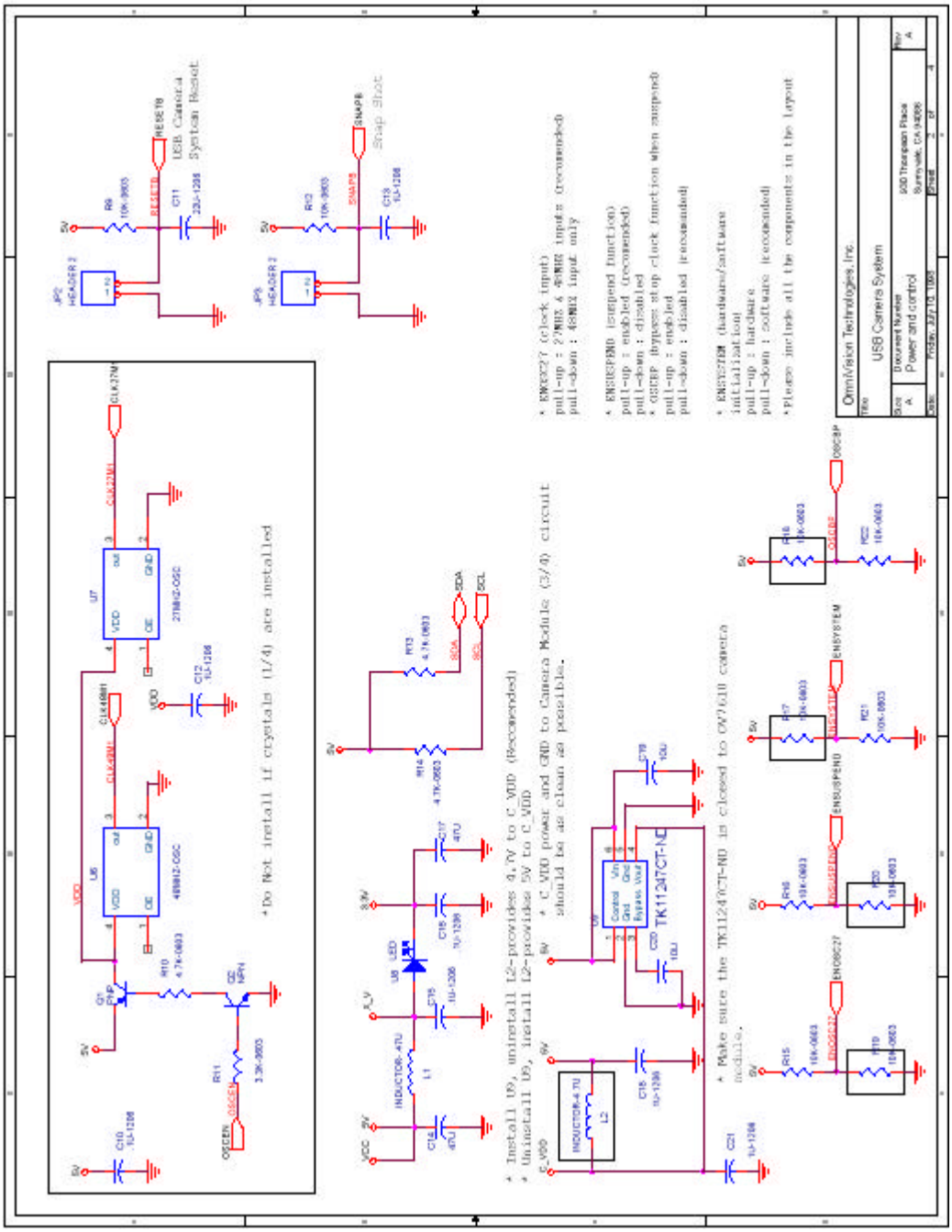
9 EVB (Evaluation Board) Design Reference

9.1 EVB Schematic Diagram

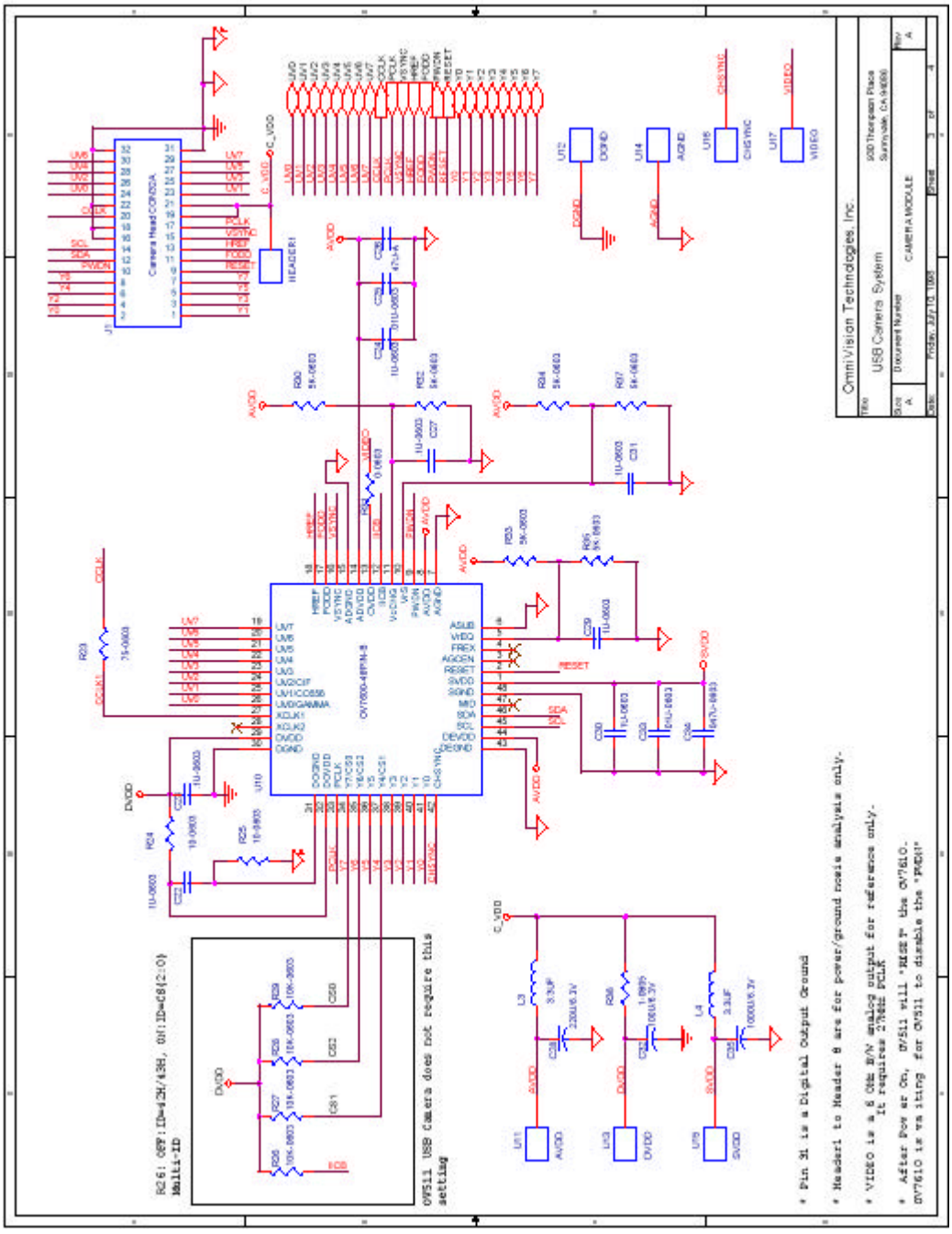
9.1.1 Page 1, OV511



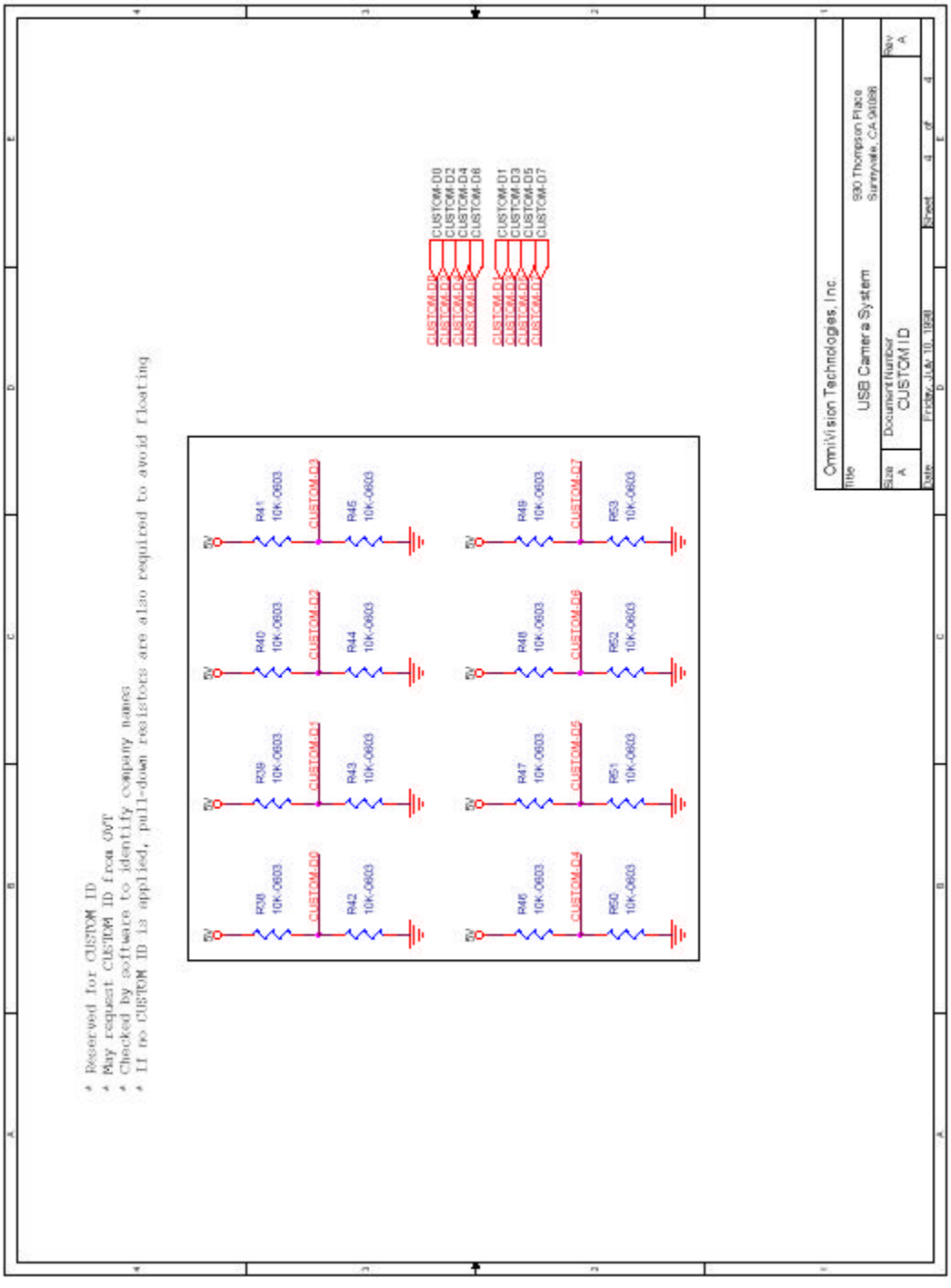
9.1.2 Page 2, Power and Control



9.1.3 Page 3, Camera Module



9.1.4 Page 4, CUSTOM ID



9.2 Board Description

9.2.1 Power Planes

The USB power through the USB cable is quite noisy such that it may seriously influence the performance of cameras. Therefore, the power planes of the USB camera system needs to be separated very carefully.

The power planes of the USB camera system can roughly partitioned as three portions,

- The power plane of the USB connector, OV511 & DRAM (5V)
- The power plane of the USB transceiver (3.3V)
- The power plane of the camera (4.7/5V)

Figure 18. Power Planes of the USB Camera System

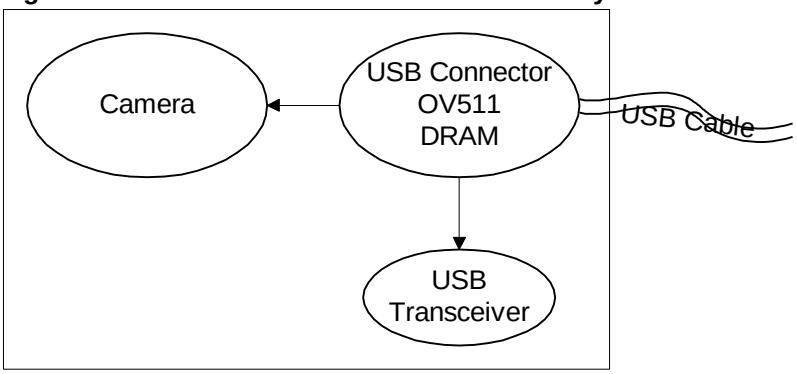
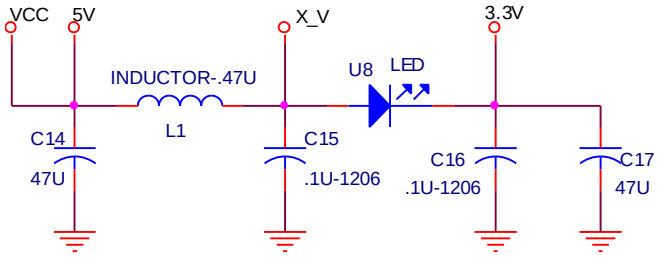


Figure 19. The Power Circuit of the USB Connector, OV511, DRAM & the USB transceiver



9.2.1.1 The Power Plane of the USB Connector, OV511 & DRAM (5V)

- 5V/VCC

5V, USB bus power from the USB connector. Supplies OV511 & DRAM.

- X_V

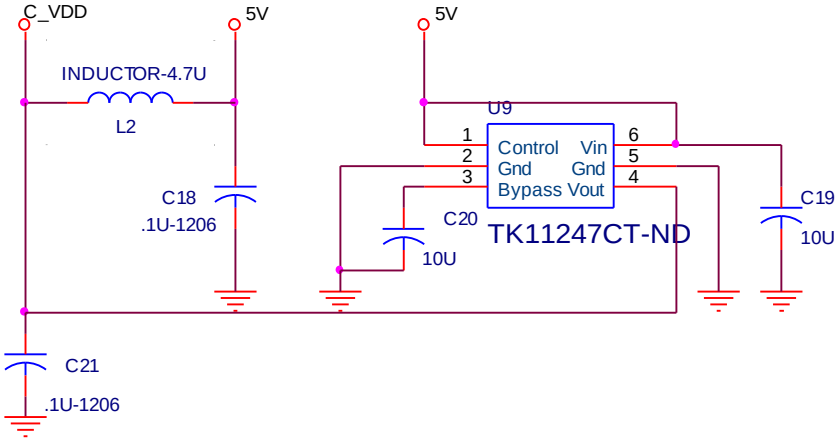
5V, intermediate power between USB bus power and 3.3V. Use a LC filter to reduce coupling of USB transition noise. Not connected to any active component.

9.2.1.2 The Power Plane of the USB Transceiver (3.3V)

- 3.3V

3.3V, USB transceiver power. Voltage drops from 5V to 3.3V simply by using a LED or it may also be generated by a 3.3V power regulator to get cleaner power.

Figure 20. The Power Circuit of the Camera



9.2.1.3 The Power Plane of the Camera (4.7/5V)

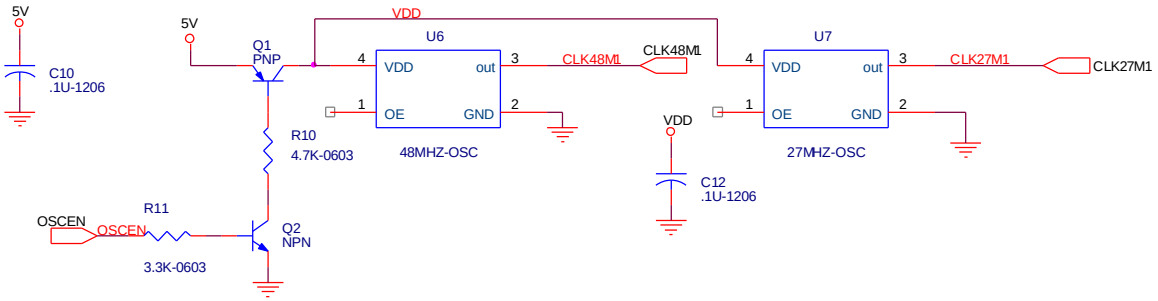
- C_VDD

4.7V/5V, camera power. Two options,

1. May use a low dropout voltage regulator, such as TOKO TK11247 or TK11447, to supply 4.75V or 4.7V to the camera.
2. May use only an inductor to bypass USB bus power if there is any noise reduction circuit for power supply on the camera board.

The power plane of the camera has to be as clean as possible.

Figure 21. The Power Circuit of Oscillators (Option)



9.2.1.4 The Power Plane of Oscillators (Option)

If crystals are installed on the USB camera system, oscillators are not required.

- VDD

5V, oscillator power controlled by pin “OSCEN”. If pin “OSCBP” is pulled down, VDD will be shut down by the power circuit (R11, Q2, R10, Q1 or simply connected to OE pin of some kinds of oscillator) when suspend occurs. If pin “OSCBP” is pulled up, VDD will never be shut down.

9.2.2 Clocks

27MHz input provides clock for camera & camera interface, while 48MHz input provides clock for USB interface. If pin “ENOSC27” is pulled up, both 27MHz & 48 MHz inputs are selected. If it is pulled down, only 48 MHz input is selected. In this case, 48 MHz input is divided by 2 to provide 24MHz clock for camera & camera interface.

Both 27MHz & 48MHz inputs may be allowed to use either crystals or oscillators. Oscillator outputs connect to pin 1 of clock buffer (CLK27M1 or CLK48M1).

9.2.3 DRAM

Only 5V EDO 256Kx16 60ns (or faster) DRAM is allowed.

9.2.4 Options

- Custom ID

The 8-bit custom ID is checked by the software to identify company names. It may be requested directly from OVT. The registered custom ID can be coded by pulling up or down resistors. If no custom ID is applied, pull-up/down resistors are also requested to avoid floating.

- ENOSC27

27MHz clock input select
Pull-up, both 27MHz & 48 MHz inputs are selected (recommended)
Pull-down, only 48 MHz input is selected

- ENSUSPEND

Hardware suspend enabled/disabled
Pull-up enable suspend function (recommended)
Pull-down, disable suspend function

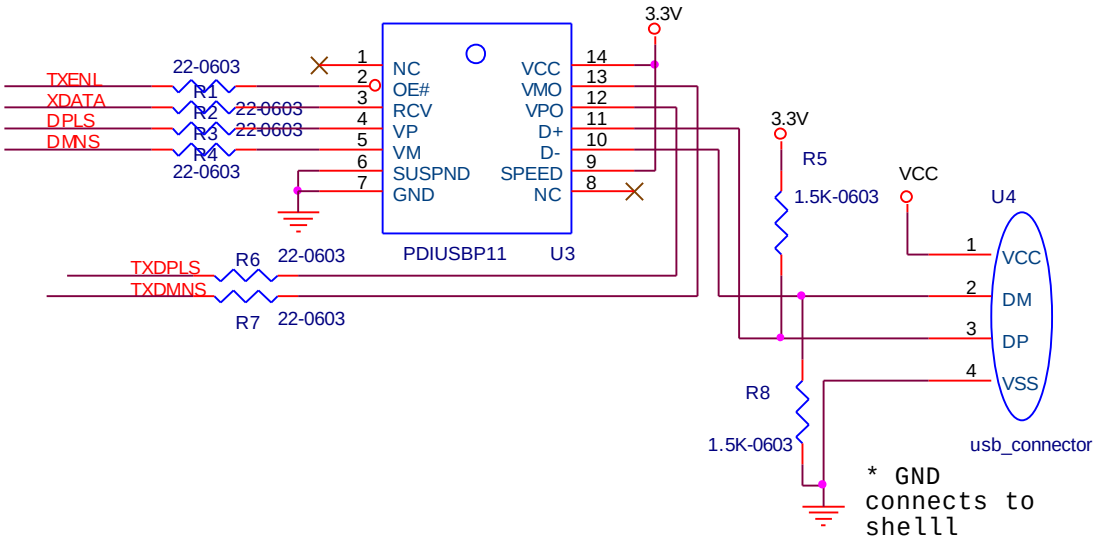
- ENSYSTEM

Hardware system initialization enabled/disabled
Pull-up system initialized by hardware
Pull-down system initialized by software (recommended)

- OSCBP

OSCEN enabled/disabled
Pull-up enabled
Pull-down disabled (recommended)

Figure 22. Circuits of Damping Resistors & Shell Grounding



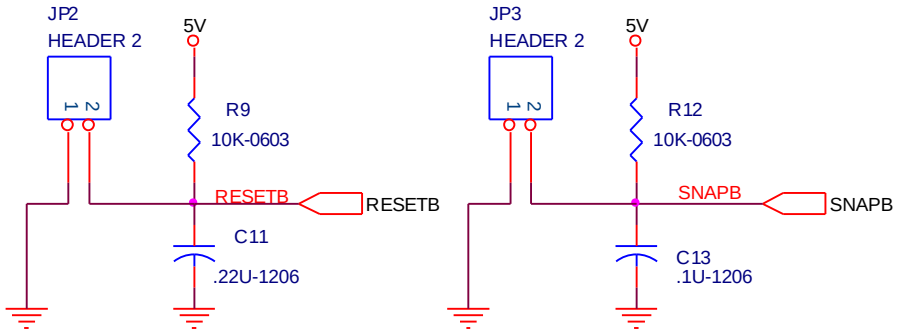
- Damping resistors & shell grounding

There are 6 signals connected to the USB transceiver, TXENL, XDATA, DPLS, DMNS, TXDPLS & TXDMNS. Damping resistors may be connected between OV511 & USB transceiver to reduce over-shot & under-shot.
Shell grounding is necessary for the USB connector.

- Switching power supply

CLK24K is a 24KHz clock output reserved for switching power supply. It is an option to reduce noise of USB transition on the power plane.

Figure 23. Circuits of Reset & Snapshot Bottoms



- Reset bottom

Pull-up resistor & pull-down capacitor provide RC constant during initialization of the whole system. Push reset bottom will reset OV511 as well as the camera.

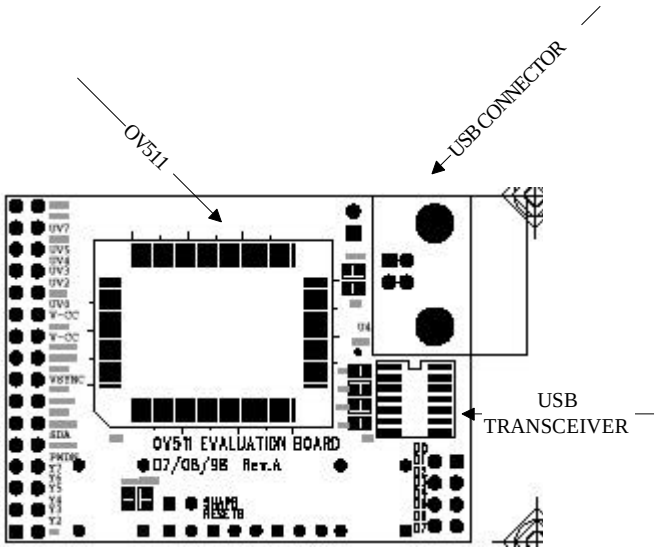
- Snapshot bottom

Push snap bottom will trigger hardware snapshot function and capture one single frame of image.

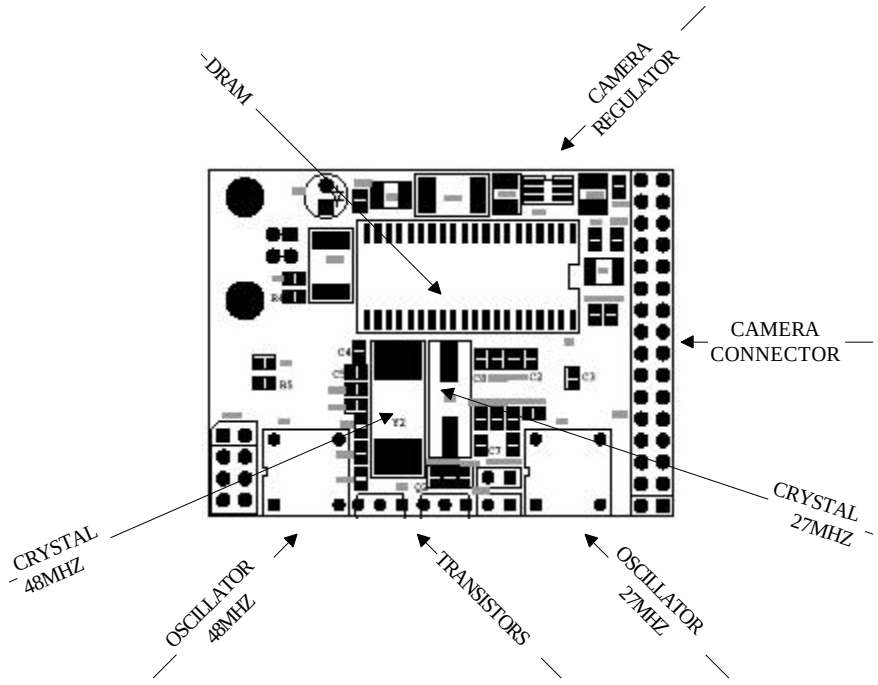
9.3 PCB Layout

9.3.1 Placement

- Top view



- Bottom view



9.3.2 Grounding

Camera ground and OV511 & DRAM ground are separated and both connected to USB ground. Shell grounding is necessary for the USB connector.

- Grounding