ZC0301

Z-Star Microelectronics Corp.

USB PC-Camera Engine / VGA Resolution

Overview

With a miniature 28-Pin PLCC package and without external DRAM, ZC0301 provides a cost effective single chip solution for PC camera application. All major image processing functions, image data compression, and data transfer units are built in the chip. The ZC0301 chip communicates with PC host via Universal Serial Bus (USB) port.

Specifications

Sensor Resolution	VGA, CIF, SIF, QCIF, QSIF
Color Process	Auto
DRAM	No Requirement
Compression	JPEG
PC Interface	USB v1.0 & v1.1
Supply Voltage	3.3v
Supply Current	100mA
Operating Temperature	0℃-50℃ (Ambient)
Package Type	28 pin PLCC

Architecture

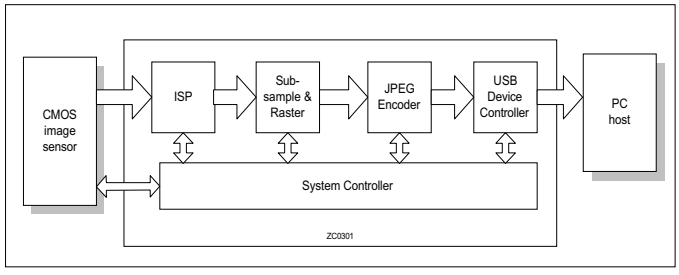

Figure 1 ZC0301 Block Diagram

Feature

- Provide most cost effective PC camera solution with 28-pin package
- Support VGA CMOS sensors from Hyundai
- Support up to 15 fps VGA and 30 fps CIF video display without DRAM
- USB Device Controller compliant with USB Protocol 1.1
- Support pan function based on 8x8 pixels unit
- Support 8-bit RGB Bayer pattern raw data input from CMOS image sensor
- Support 2-wire control interface to CMOS image sensor
- Support programmable color correction and gamma correction
- Support AE/AWB and programmable AE/AWB windows
- Support automatic CMOS Reset Level Control
- Support automatic Gain Control
- Support auto/manual Histogram Equalization
- Support 2x2 Sub-Sampling
- Support ISO/IEC 10918-1 (JPEG) standard image compression
- Support JPEG File Interchange Format (JFIF) compressed image data output
- Support 2 AC and 2 DC Huffman code table
- Support 4 quantization tables for programmable image quality
- Adjustable compression ratio
- Support Custom-ID option

Figure 2 Chip Pin Out Diagram

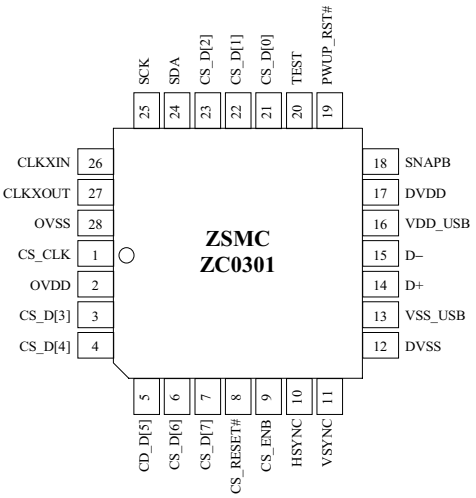

Table 1 ZC0301 Chip Pin Out

Signal	Function	Type	28PLCC Pin #
CS_CLK	Sensor clock	O	1
OVDD	I/O power	P	2
CS_D[3]	Sensor data	I/O, PD	3
CS_D[4]	Sensor data	I/O, PD	4
CS_D[5]	Sensor data	I/O, PD	5
CS_D[6]	Sensor data	I, PD	6
CS_D[7]	Sensor data	I, PD	7
CS_RESET#	Sensor reset	O	8
CS_ENB	Sensor power enable	I/O	9
HSYNC	Horizontal sync	I, PD	10
VSYNC	Vertical sync	I, PD	11
DVSS	Core ground	P	12
VSS_USB	USB transceiver ground	P	13
D+	USB Data	I/O	14
D-	USB Data	I/O	15
VDD_USB	USB transceiver power	P	16
DVDD	Core power	P	17
SNAPB	Snap	I, PU	18
PWUP_RST#	Power-on reset	I, Schmitt	19
TEST	Manufacturing test enable	I, PD	20
CS_D[0]	Sensor data	I, PD	21
CS_D[1]	Sensor data	I, PD	22
CS_D[2]	Sensor data	I, PD	23
SDA/ESDA	IIC/EEPROM data	I/O, Schmitt	24
SCK/ESCK	IIC/EEPROM clock	O	25
CLKXIN	Crystal input	I	26
CLKXOUT	Crystal output	O	27
OVSS	I/O ground	P	28

Notes: P -- Power pad PD -- Internal pull-down resistor / -- Multi-function separator

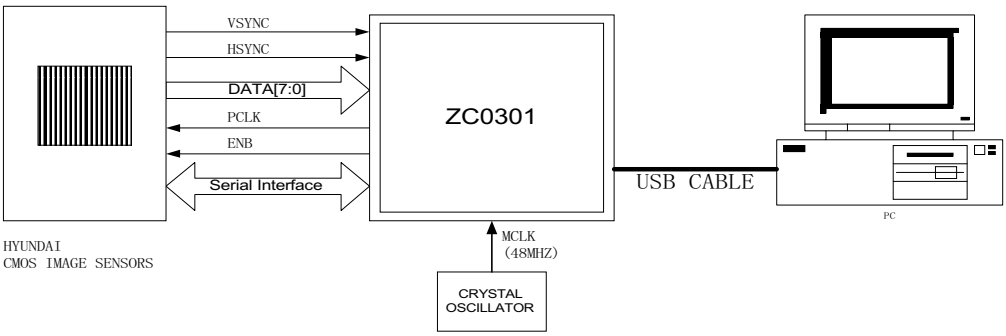

Figure 3 USB PC Camera System Block Diagram

Technical Description

The ZC0301 consists of five major function blocks, *System Controller, Image Signal Processor, Sub-Sample & Raster, JPEG Encoder,* and *USB Device Controller,* as illustrated in Figure 1. These blocks provide the following functions.

System Controller

- Providing the control to ISP, JPEG, and USB blocks
- Configuring the control registers
- Chip clock generation
- Error control for the data block through USB interface

Image Signal Processor

- Dedicated sensor control and signal processing module.
- Serial-Bus interface for CMOS Image Sensor
- 8 bit Bayer format image input
- 3x3 Interpolation
- Color Correction
- Gamma Correction
- Automatic Exposure Control
- Automatic White Balance Control
- Programmable AE windows
- Automatic Reset Level Control
- RGB to YCrCb Color Space Convert
- Histogram Equalization Logic

Sub-Sample & Raster

- The input data format is 4:4:4 for Y component, Cb component and Cr component. The three components for a pixel are input simultaneously.
- The output data format is in 4:2:2 for the three components. The output sequence is Y,Y,Cb,Cr for the three components.
- When scale option is deserted, the output pixel number is the same as the input pixel number; when scale option is asserted, the output pixel number is 1/4 of the pixel number of input image.
- Change input image data format to 8x8 block data format required by DCT module.

JPEG Encoder

- Provides the register for control the image size, compression rate and the image quantity after compression. It can be configured through USB interface by the software.
- The external system controller will send the reset signal to enable or disable JPEG operation.
- There is single clock to control the data flow in JPEG module, the maximum clock frequency is 24Mhz.

USB Device Controller

- Compliant with USB protocol 1.1
- Support full speed device
- Clock and data recovery from USB
- Bit stripping/stuffing and NRZI decoder/encoder
- Check all possible error conditions, including CRC error, bit stuffing error, PID error, as well as synchronization error
- Support all standard request and vendor/class request
- Configuration can be changed easily to apply different application
- Support suspend mode

Clocking

External 48MHz input clock is generated from on board oscillator circuit. This oscillator circuit can be turned off when ZC0301 operates in low power mode triggered by USB suspend mode.

Test Access

The ZC0301 supports scan chain test access. The Unit Monitor feature provides the capability to observe the internal state of ZC0301 by bringing out selected number of critical signals from each design unit to the chip pins.

System Recovery

If the host determines that the camera state is lost, the ZC0301 and CMOS image sensor can be commanded to reset via the USB.

Electrical Characteristics

See datasheet.

Power Requirements

See datasheet

Device Package

28-pin PLCC

Z-Star Microelectronics Corporation, USA
1758 N. Shoreline Blvd.
Mountain View, CA 94043, USA
Tel: 1-650-966-1882
Fax: 1-650-966-1885

Z-Star Microelectronics Corporation, Beijing
Room 810, Haidian Science & Technology Bldg,
7A Baishiqiao Road, Haidian District,
Beijing, P. R. China, Post Code: 100081
Tel: 10-68944017
Fax: 10-68944075

www.zsmc.com